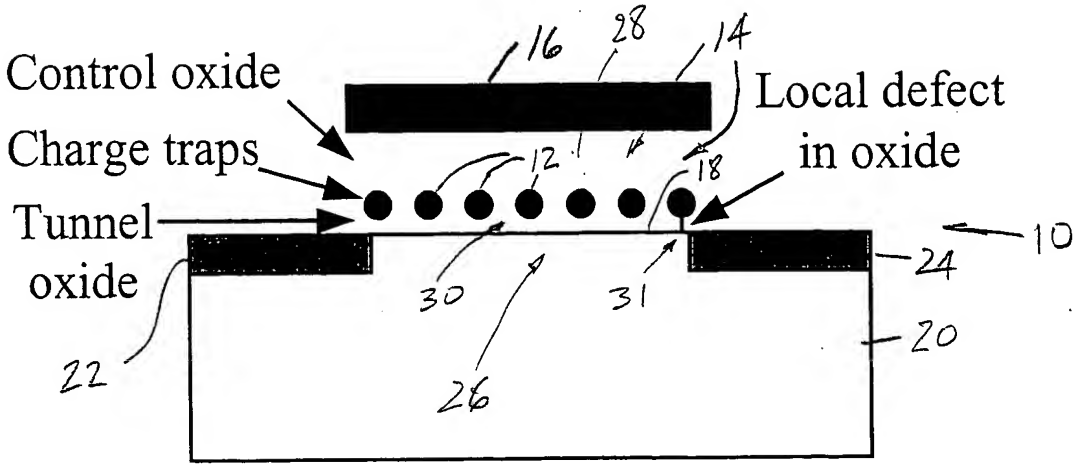
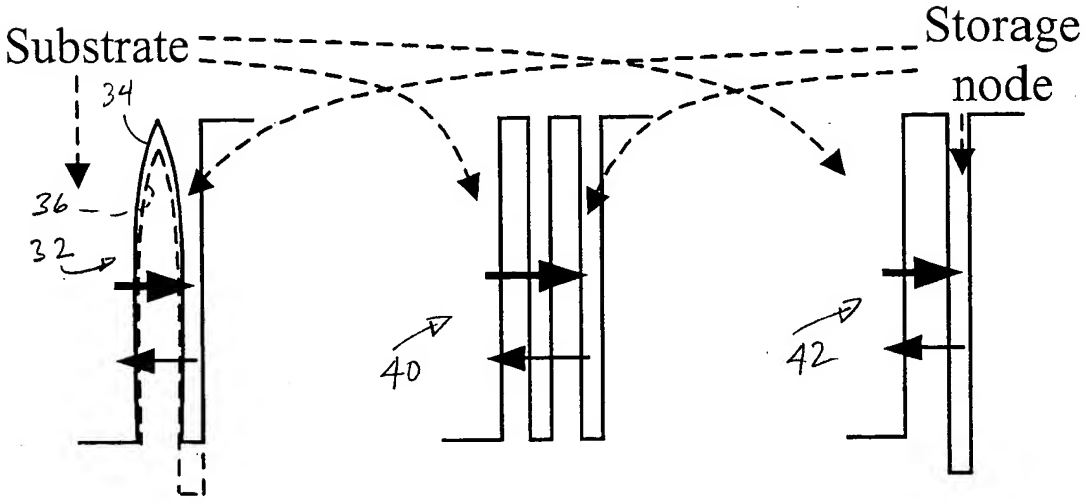


FIG. 1(a)



Dielectric Engineering

Double-stack storage nodes

Work function Engineering

FIG 1(b)

(b)

FIG 1(c)

FIG 1(d)

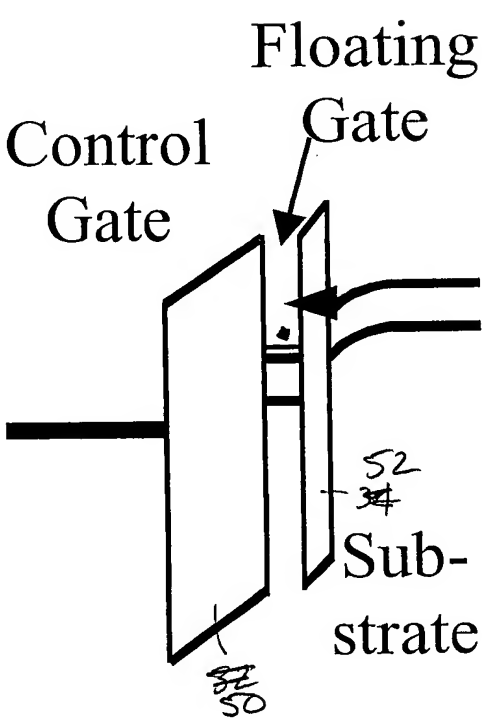


FIG. 2(a)
(writing)

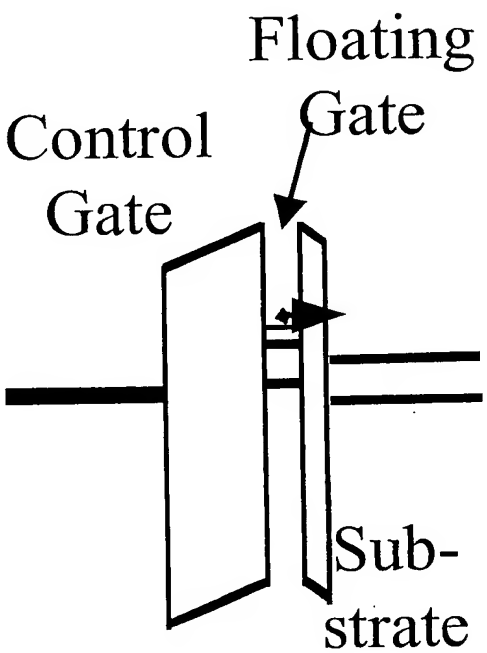


FIG. 2(b)
(retention)

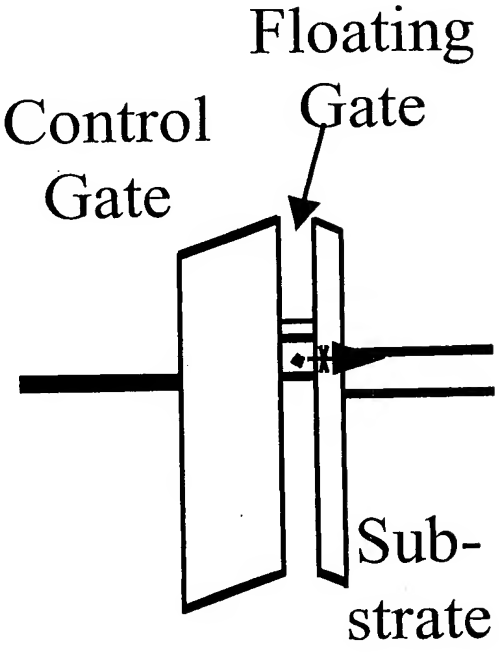


FIG. 2(c)
(retention)

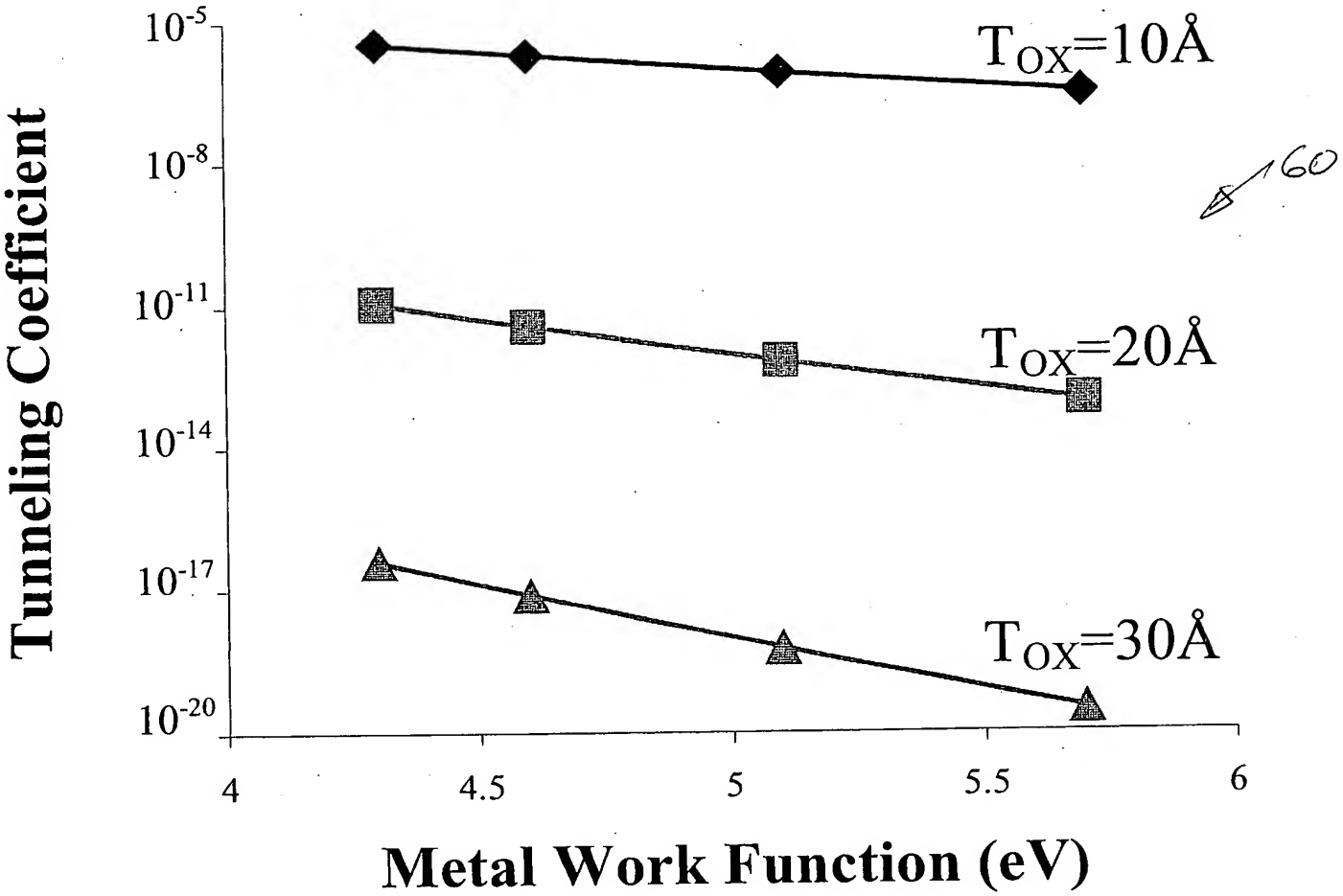

Tunneling Coefficient
10-5
10-8
10-11
10-14
10-17
10-20
TOX=10Å
TOX=20Å
TOX=30Å
160
4
4.5
5
5.5
6
Metal Work Function (eV)

FIG. 3

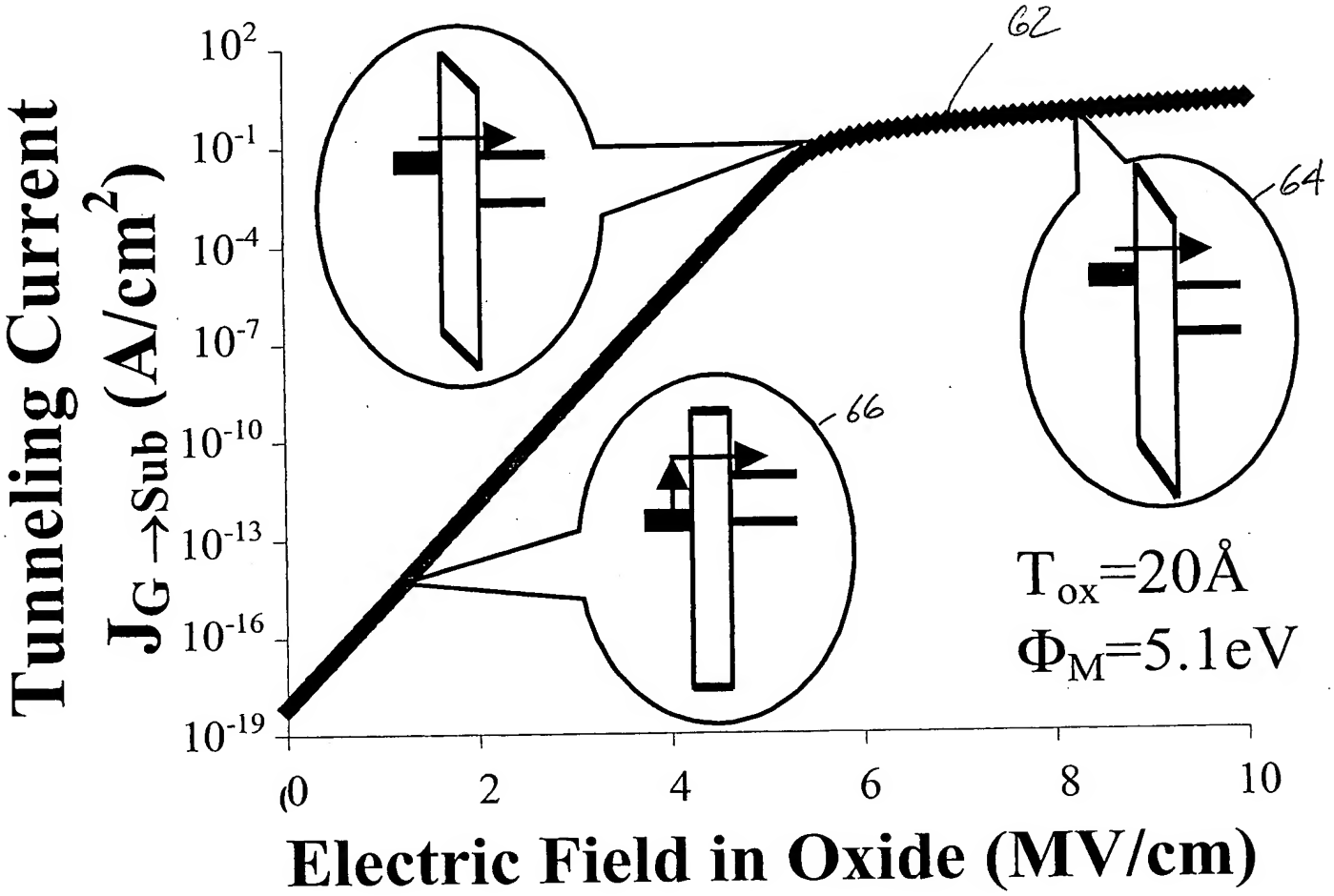

Tunneling Current
$J_{G \rightarrow Sub}$ (A/cm^2)
10^{2}
10^{-1}
10^{-4}
10^{-7}
10^{-10}
10^{-13}
10^{-16}
10^{-19}
0
2
4
6
8
10
Electric Field in Oxide (MV/cm)
62
64
66
T_{ox}=20Å
Φ_M=5.1eV

FIG. 4

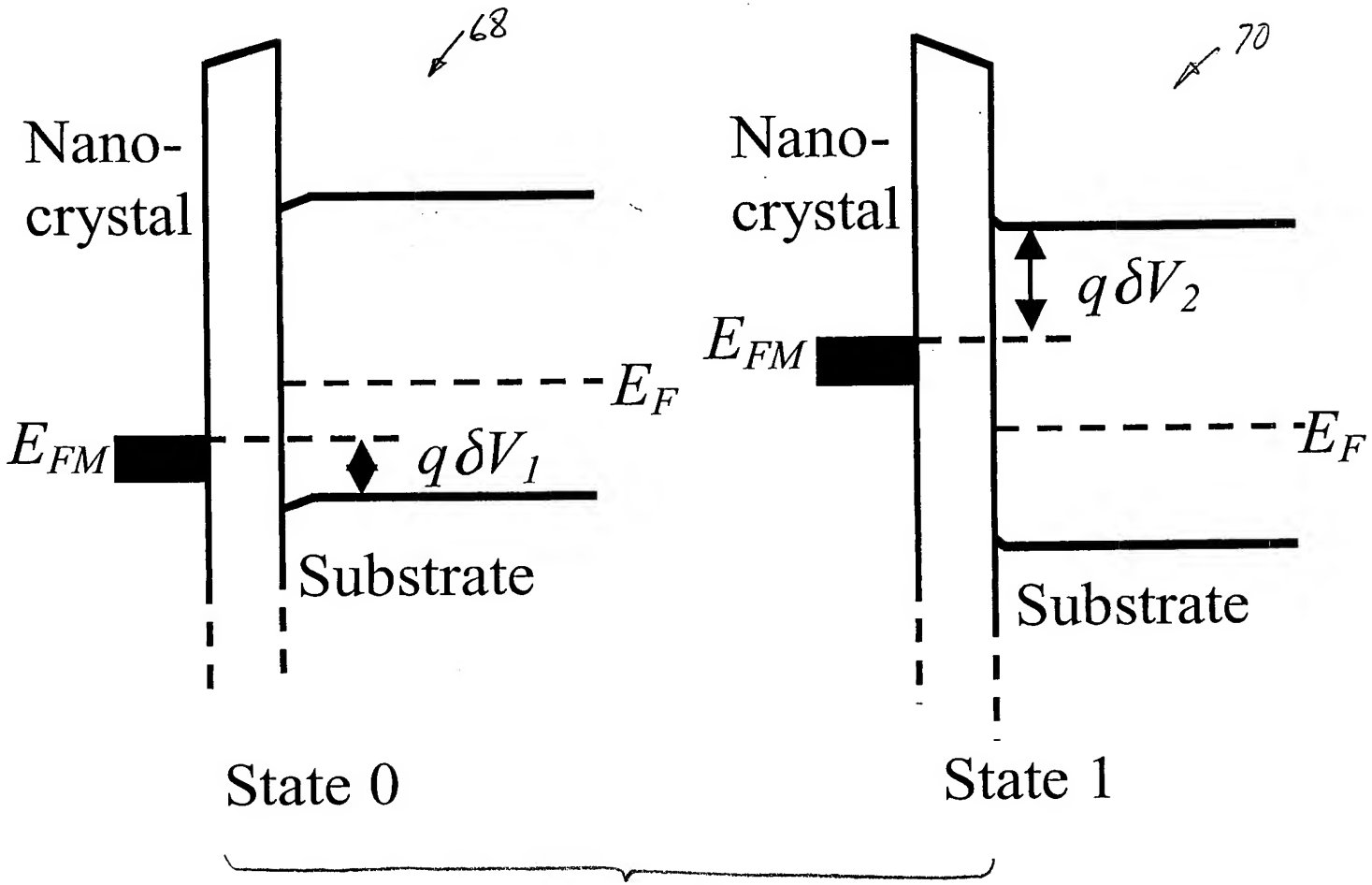

68
Nano-
crystal
E_F
E_{FM}
$q\delta V_1$
Substrate
State 0
70
Nano-
crystal
$q\delta V_2$
E_{FM}
E_F
Substrate
State 1

FIG. 5

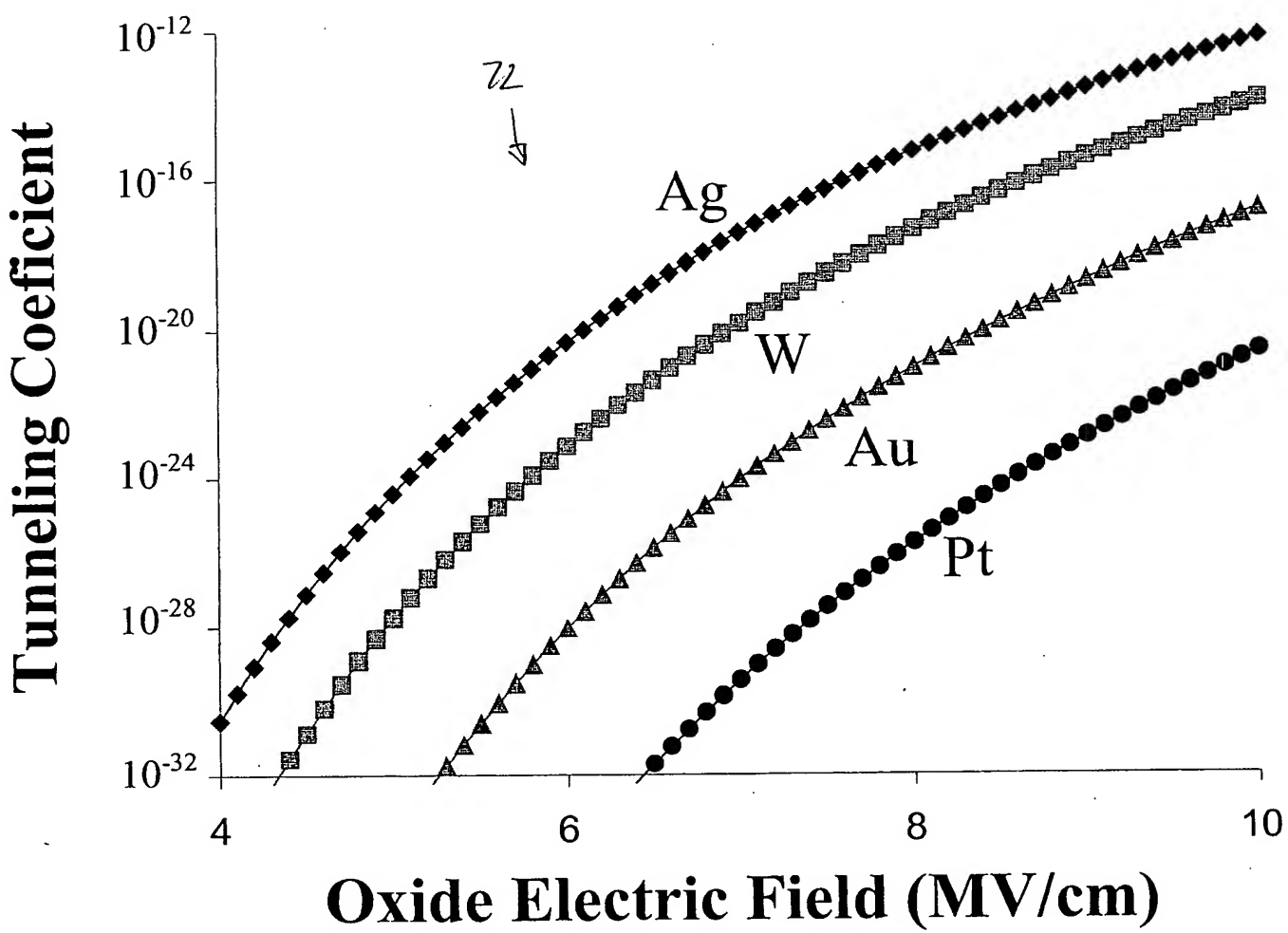

Tunneling Coeficient
10-12
10-16
10-20
10-24
10-28
10-32
22
Ag
W
Au
Pt
4
6
8
10
Oxide Electric Field (MV/cm)

FIG. 6

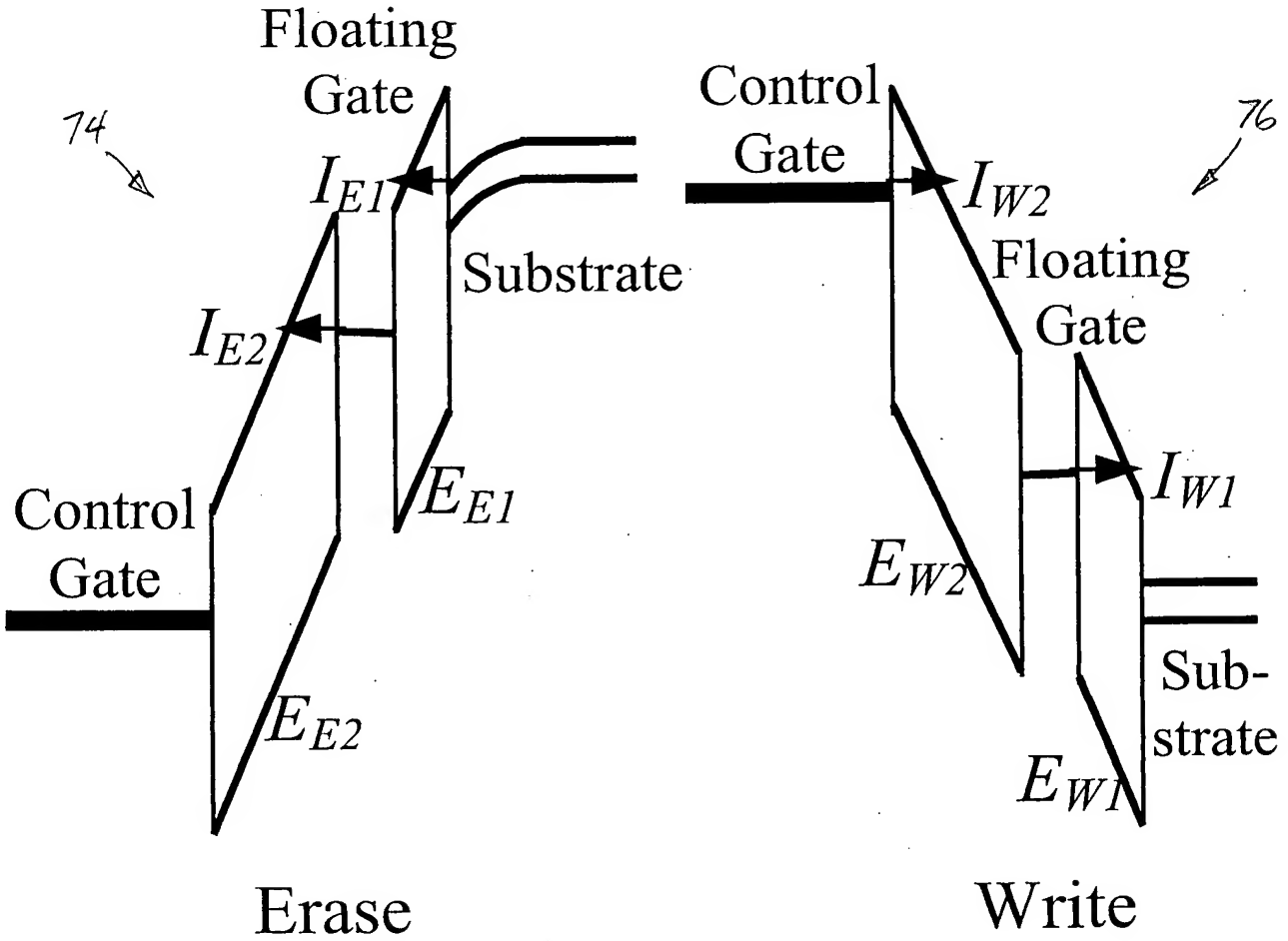

74
Floating Gate
I_{E1}
Substrate
I_{E2}
Control Gate
E_{E1}
E_{E2}
Erase
76
Control Gate
I_{W2}
Floating Gate
I_{W1}
E_{W2}
Sub-strate
E_{W1}
Write

FIG. 7

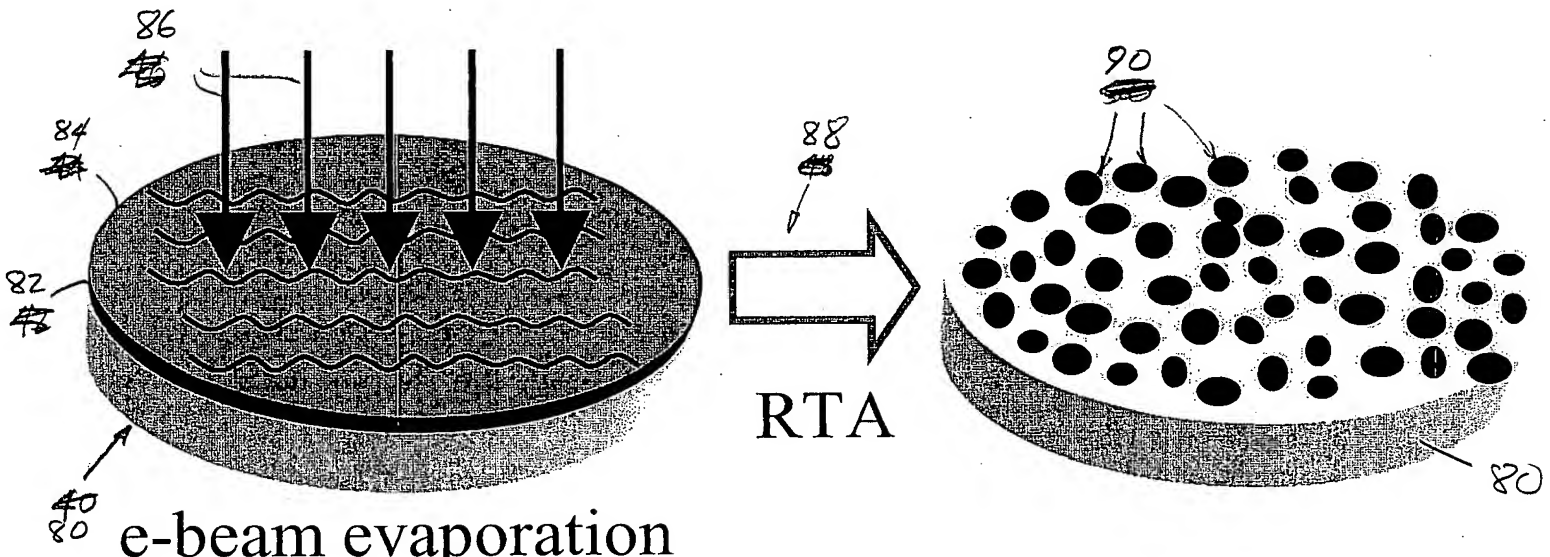

86
84
82
40
80
88
RTA
90
80
e-beam evaporation
of thin metal film

FIG 8

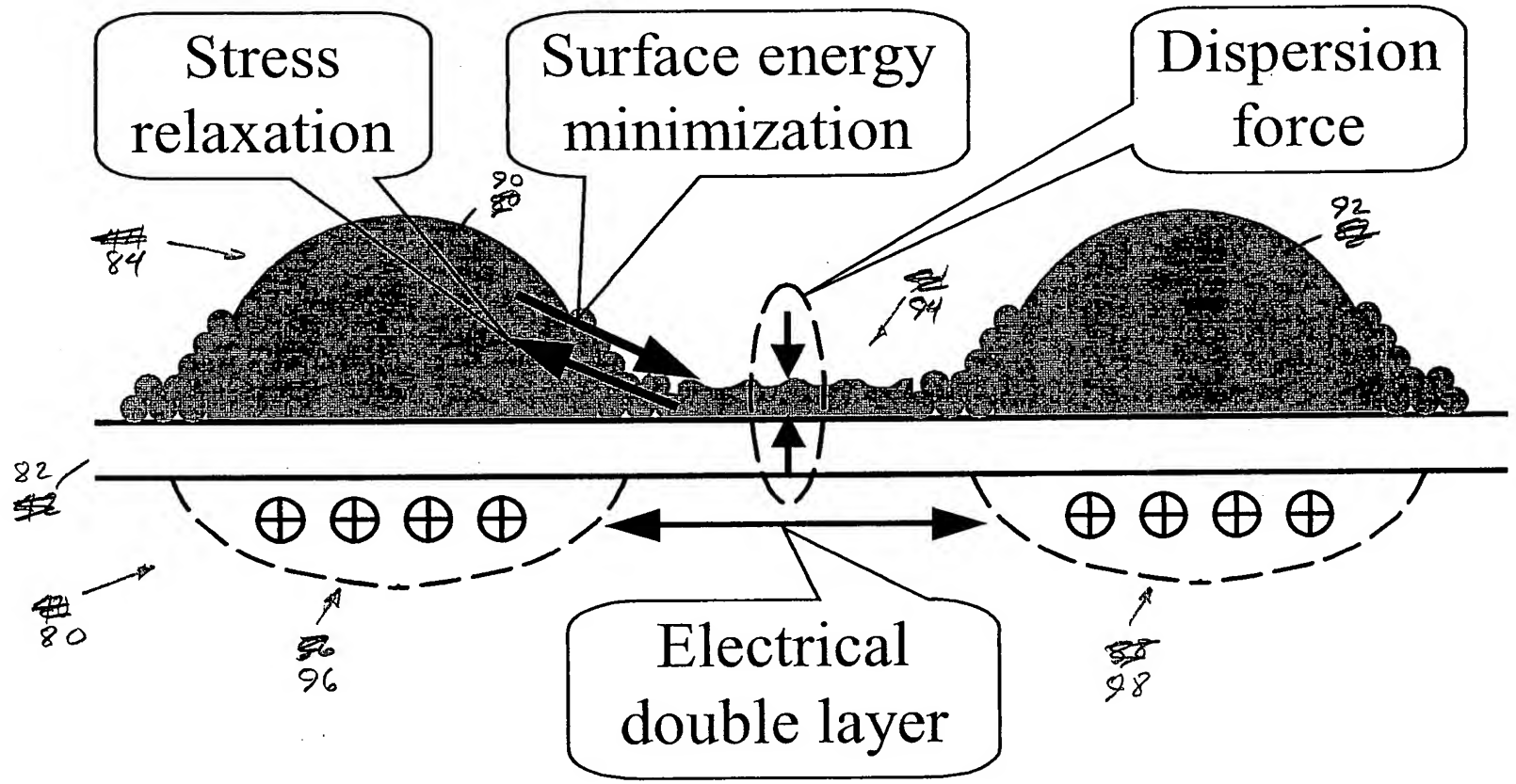

Stress relaxation
Surface energy minimization
Dispersion force
90
92
84
94
82
80
96
98
Electrical double layer

FIG. 9

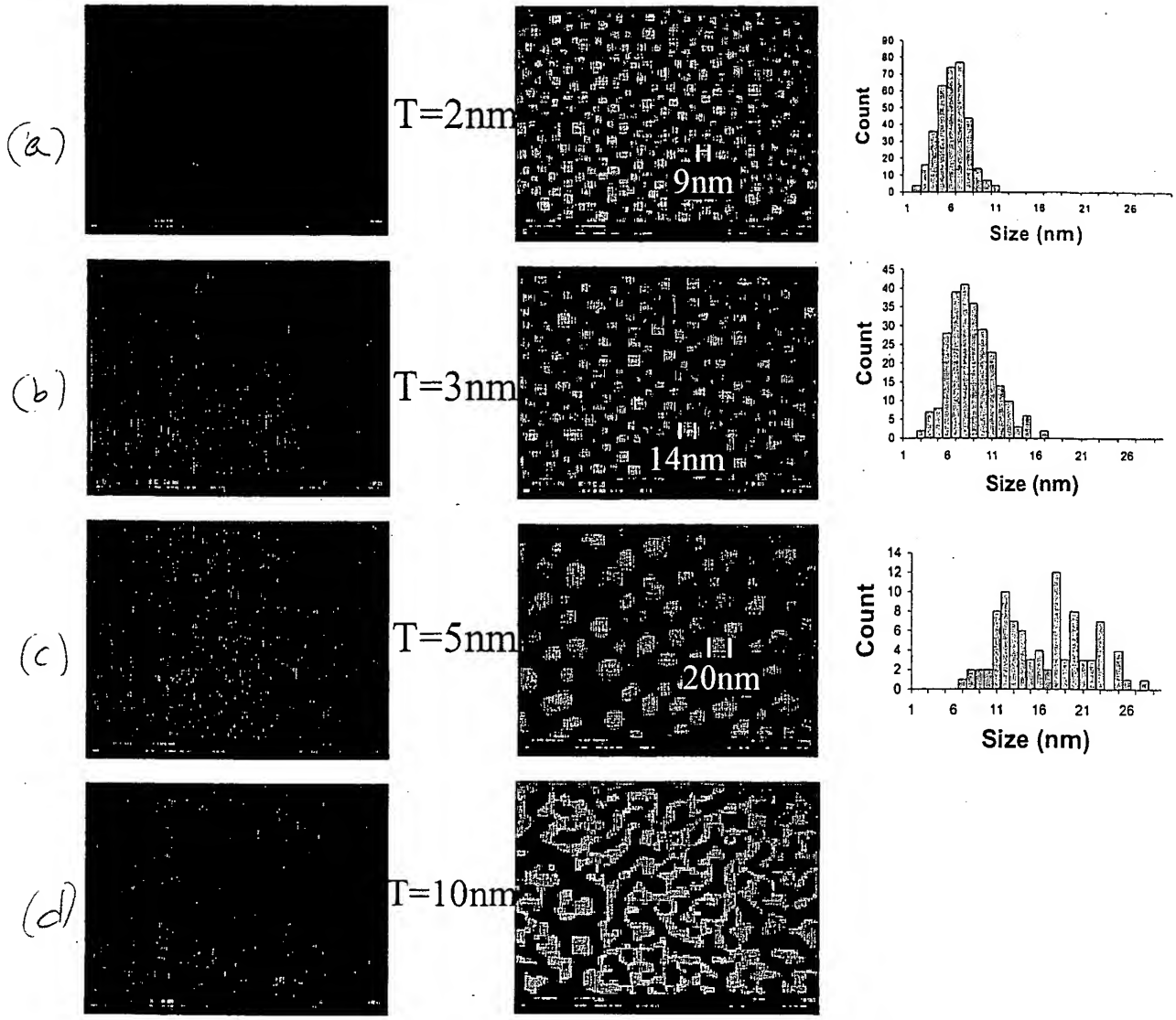
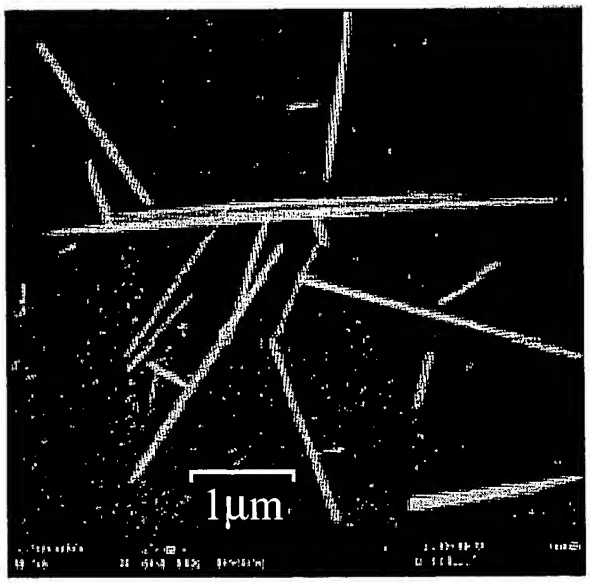

(a)
T=2nm
9nm
Count
Size (nm)
(b)
T=3nm
14nm
Count
Size (nm)
(c)
T=5nm
20nm
Count
Size (nm)
(d)
T=10nm
Before RTA
After RTA
Size Distribution

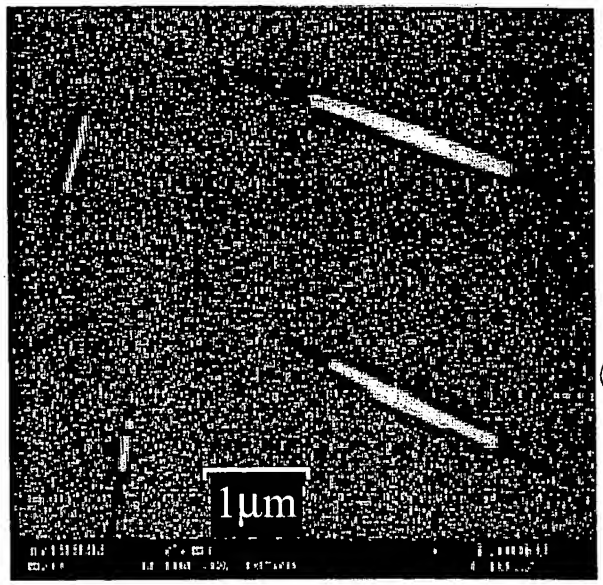
FIG. 10

(a)



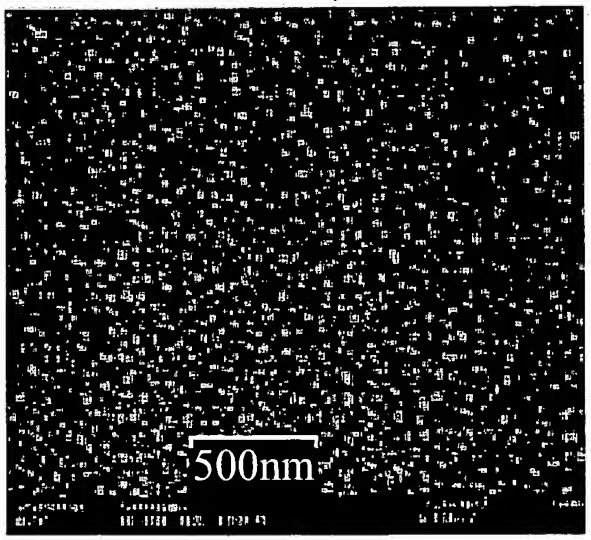
RTA at 950°C, 2 minutes

(b)



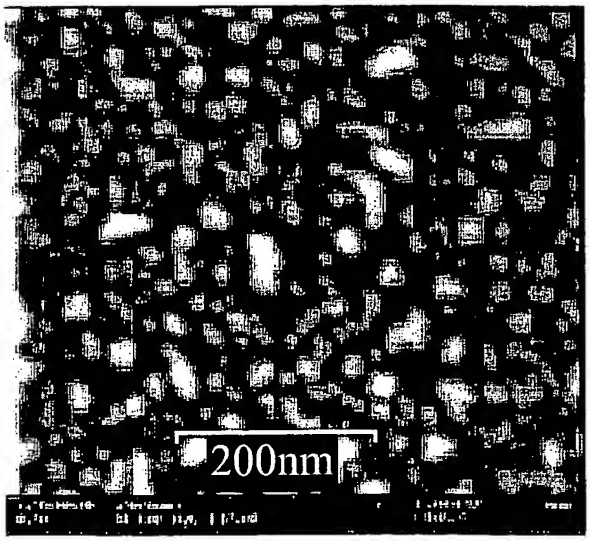
RTA at 1000°C, 2 minutes

(c)



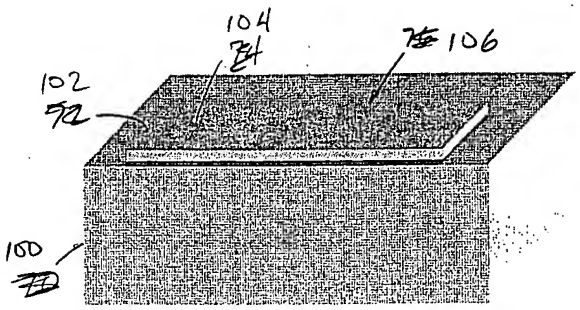
RTA at 1050°C, 2minutes

(d)

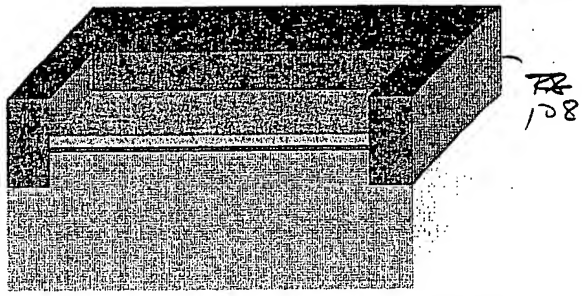


RTA at 1100°C, 2 minutes

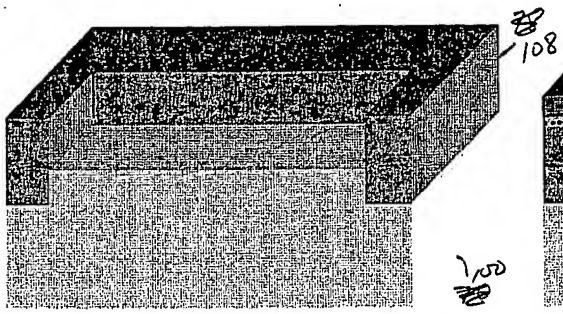
FIG. 11



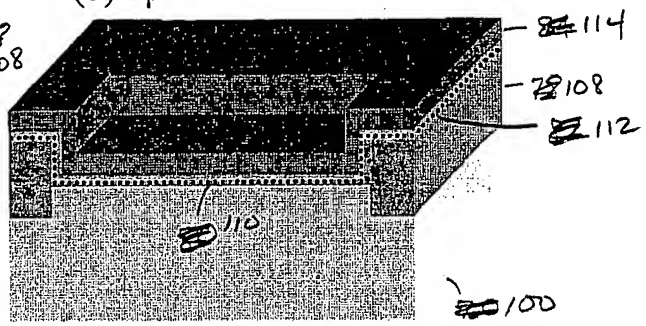
(a) Definition of active region



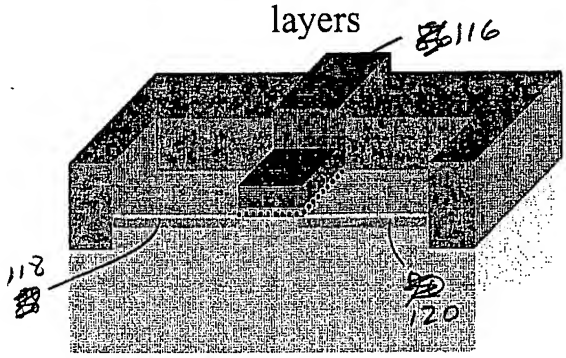
(b) 1μm field oxidation



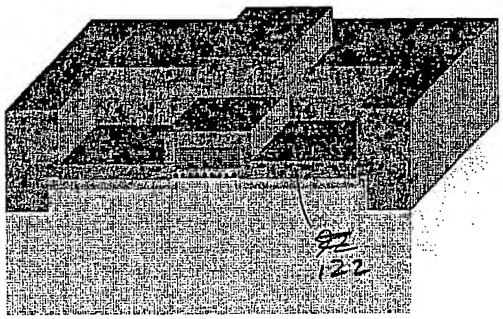
(c) Stripping nitride and pad oxide layers



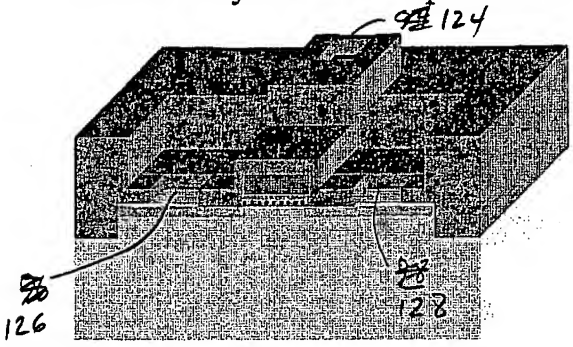
(d) Gate stack formation



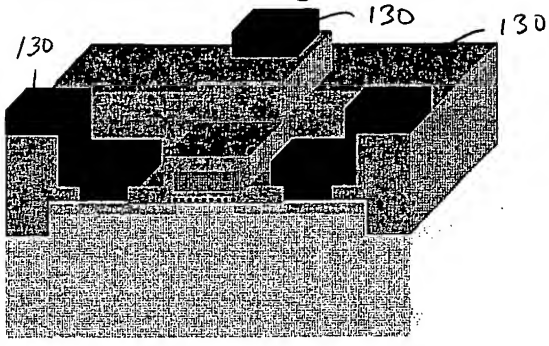
(e) Definition of gate pattern followed by S/D ion implantation



(f) PECVD oxide deposition for isolation between gate and S/D



(g) Etching contact window



(h) W sputtering and etching for final metalization

FIG. 12

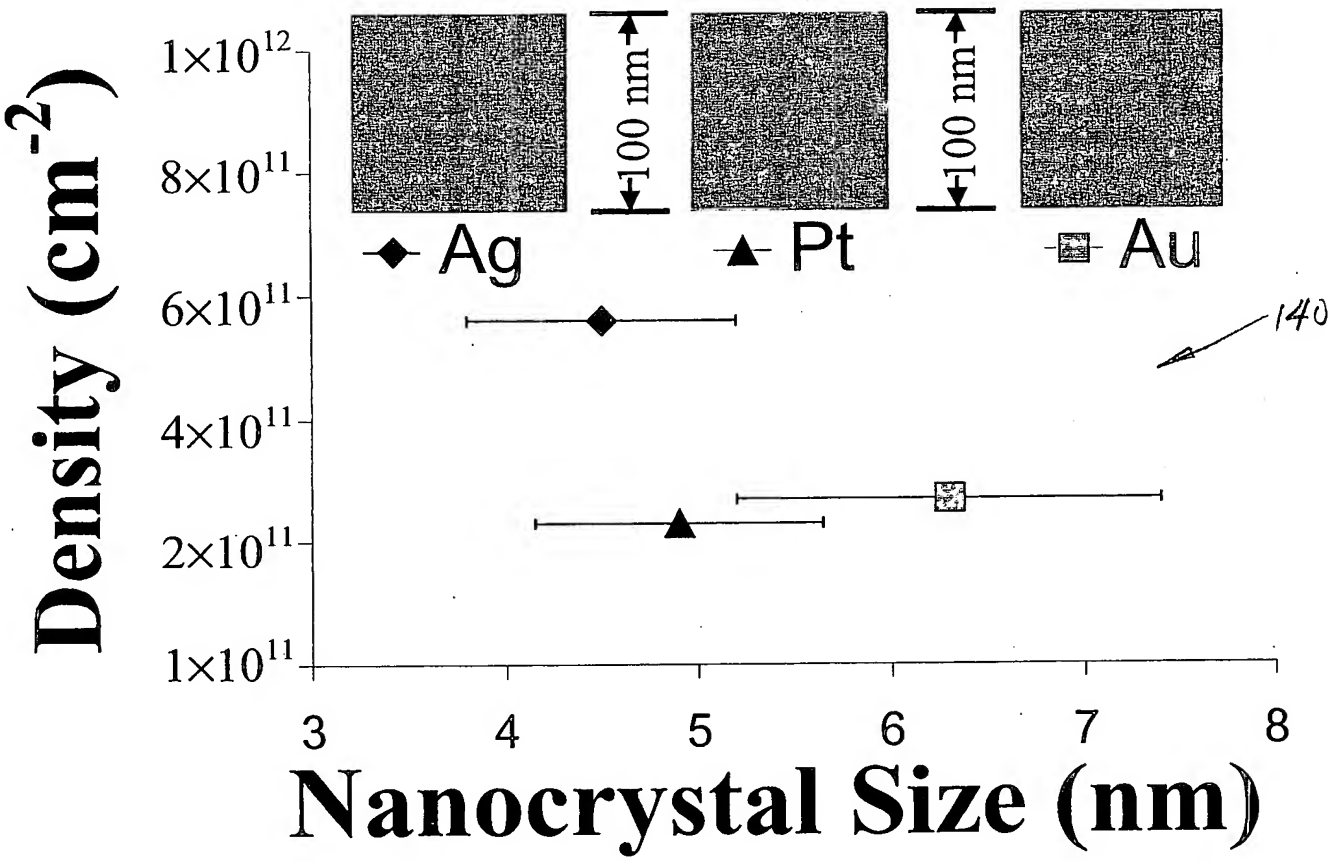

Density (cm^{-2})
1×10^{12}
8×10^{11}
6×10^{11}
4×10^{11}
2×10^{11}
1×10^{11}
100 nm
100 nm
Ag
Pt
Au
140
3
4
5
6
7
8
Nanocrystal Size (nm)

FIG 13

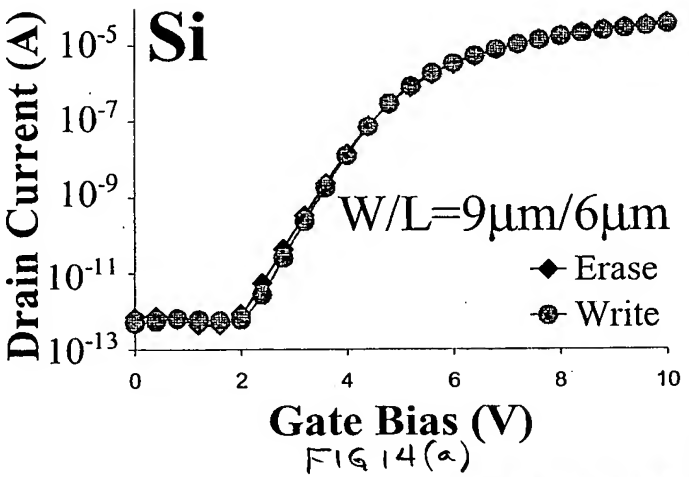


FIG 14(a)

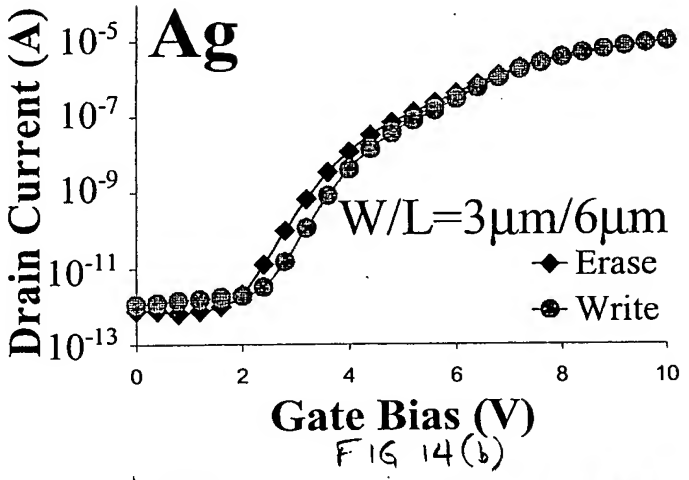


FIG 14(b)

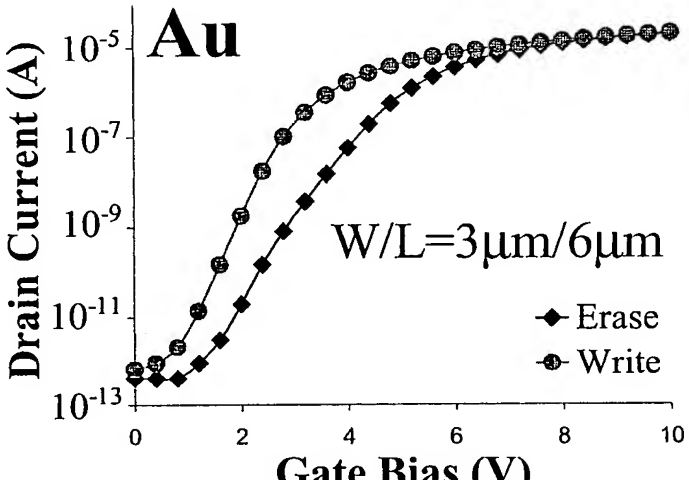


FIG 14(c)

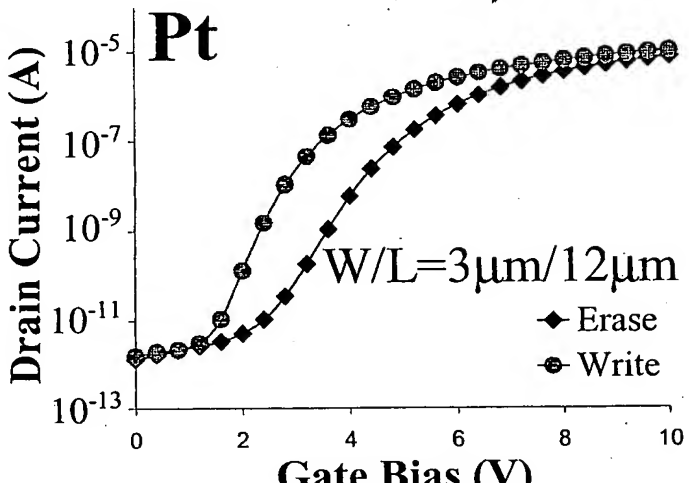


FIG 14(d)

~~FIG 14~~

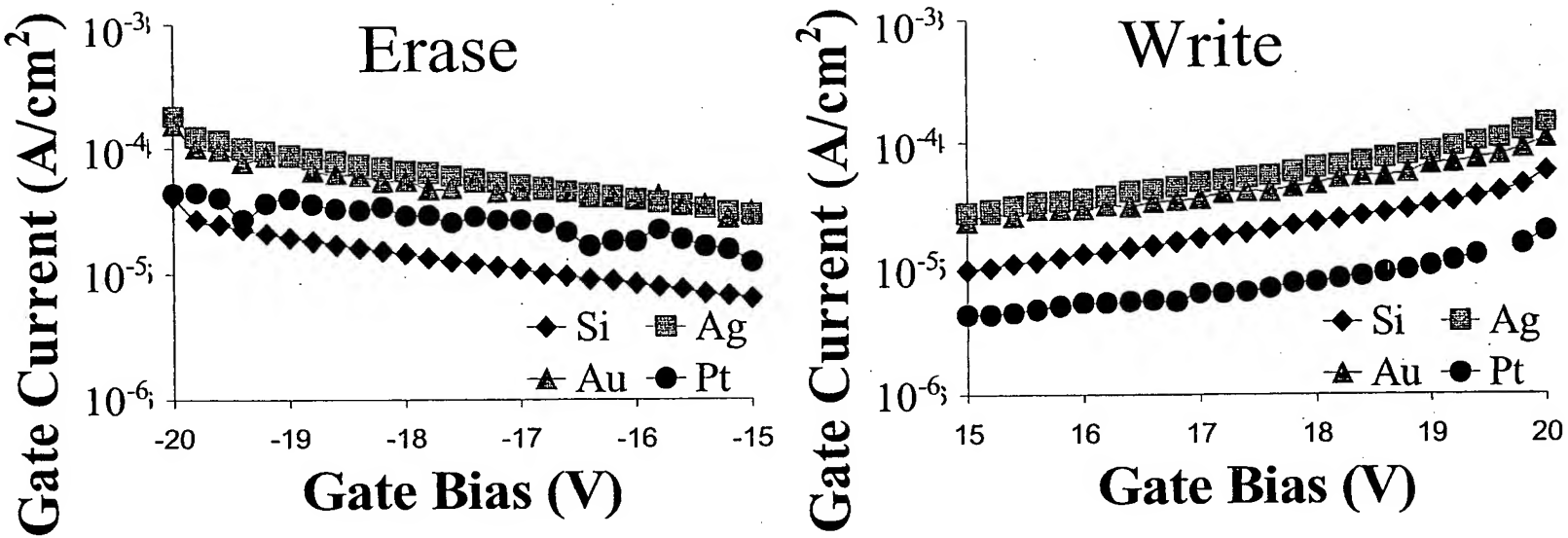

Erase
Gate Current (A/cm^2)
10^{-3}
10^{-4}
10^{-5}
10^{-6}
-20
-19
-18
-17
-16
-15
Gate Bias (V)
Si
Ag
Au
Pt
Write
Gate Current (A/cm^2)
10^{-3}
10^{-4}
10^{-5}
10^{-6}
15
16
17
18
19
20
Gate Bias (V)
Si
Ag
Au
Pt

FIG. 15

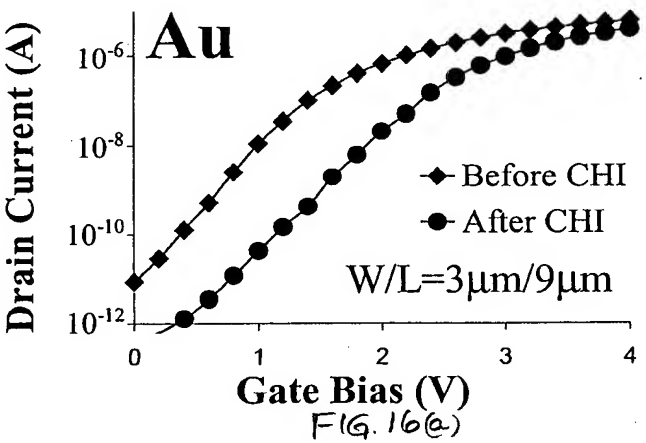


FIG. 16(a)

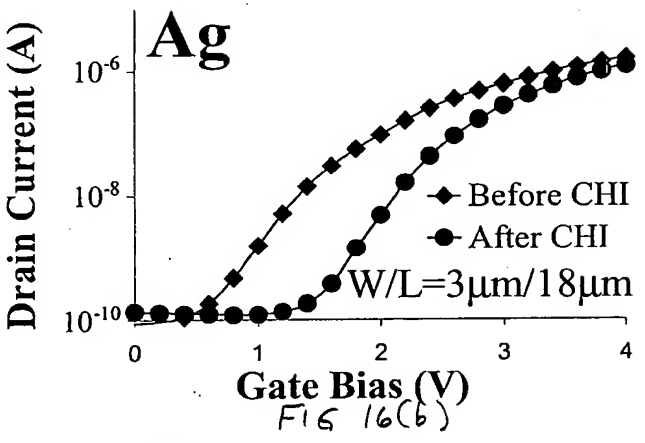


FIG 16(b)

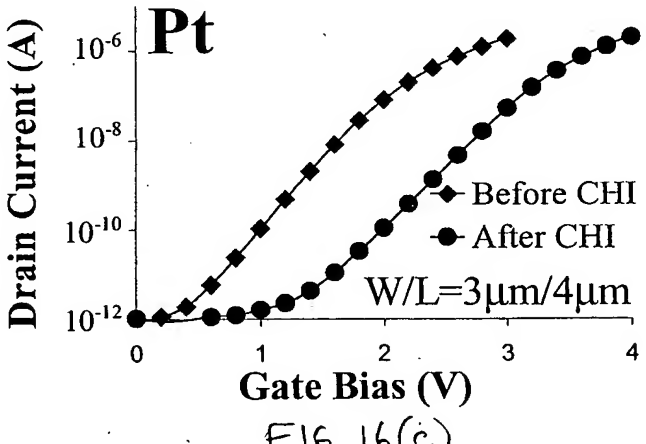


FIG 16(c)

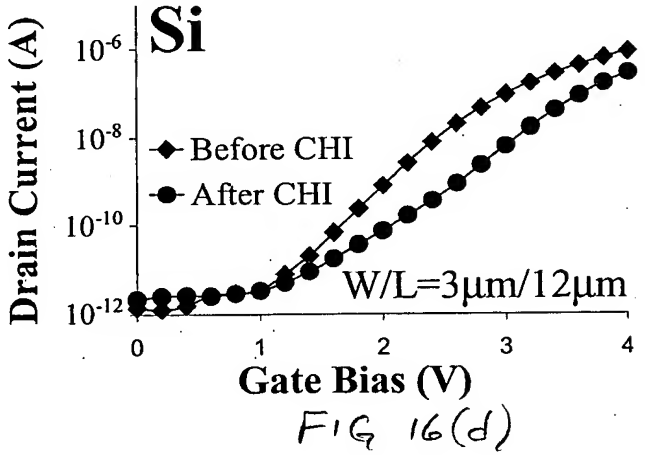


FIG 16(d)

FIG 16

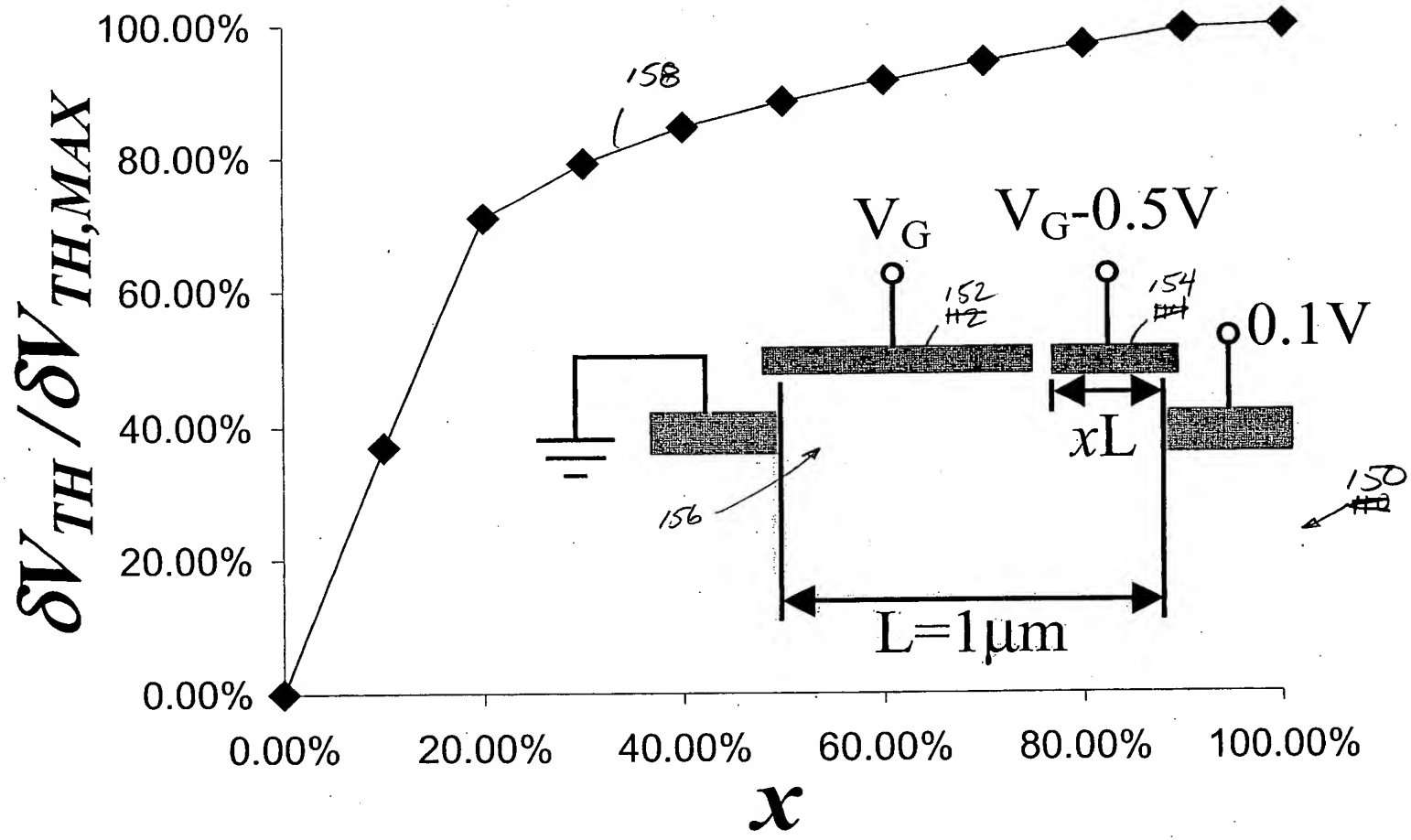

100.00%
80.00%
60.00%
40.00%
20.00%
0.00%
0.00%
20.00%
40.00%
60.00%
80.00%
100.00%
$\delta V_{TH} / \delta V_{TH,MAX}$
x
158
V_G
V_G-0.5V
0.1V
152
154
150
156
xL
L=1μm

FIG 17

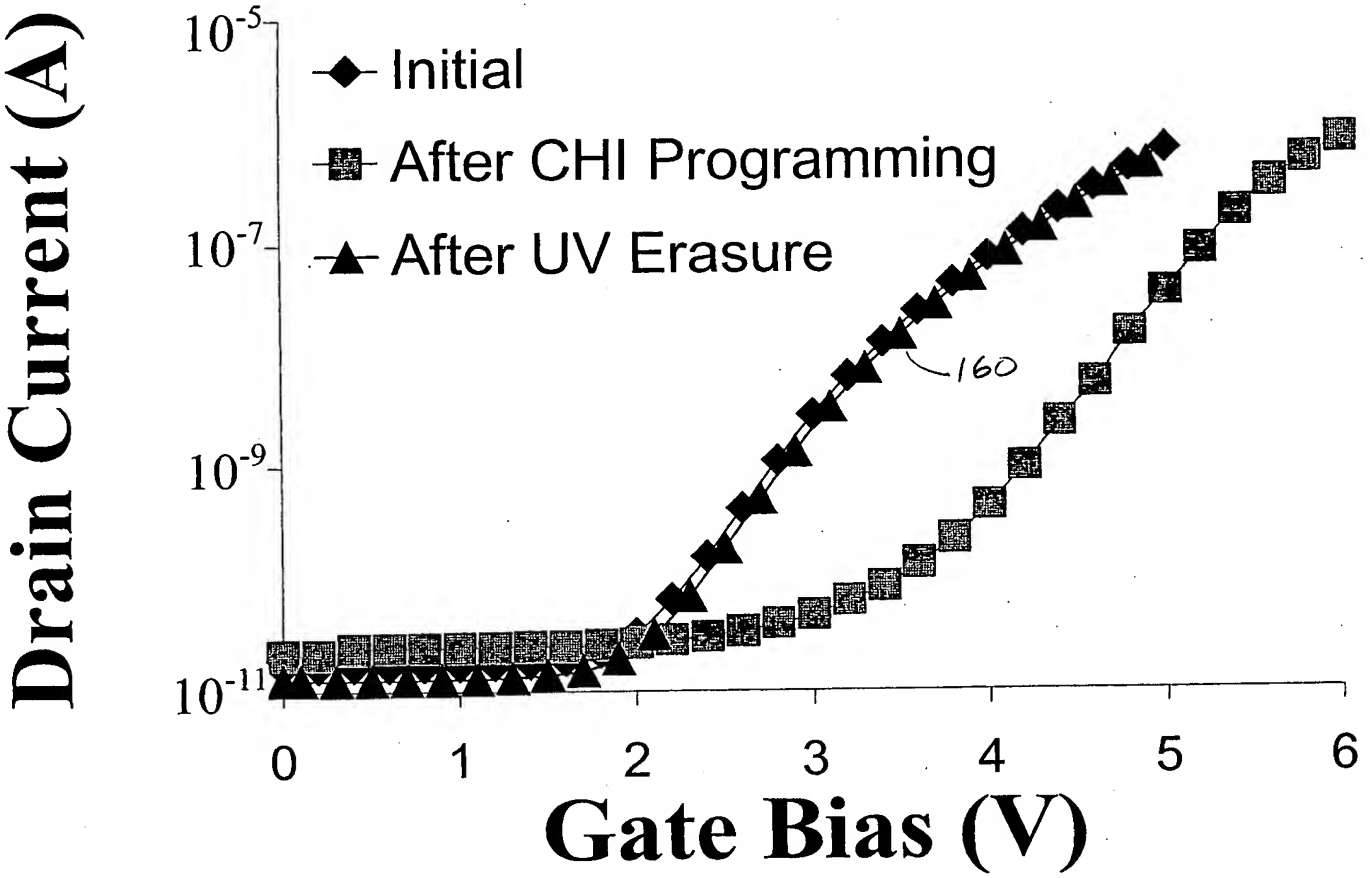

Drain Current (A)
10-5
10-7
10-9
10-11
Initial
After CHI Programming
After UV Erasure
160
0
1
2
3
4
5
6
Gate Bias (V)

FIG 18

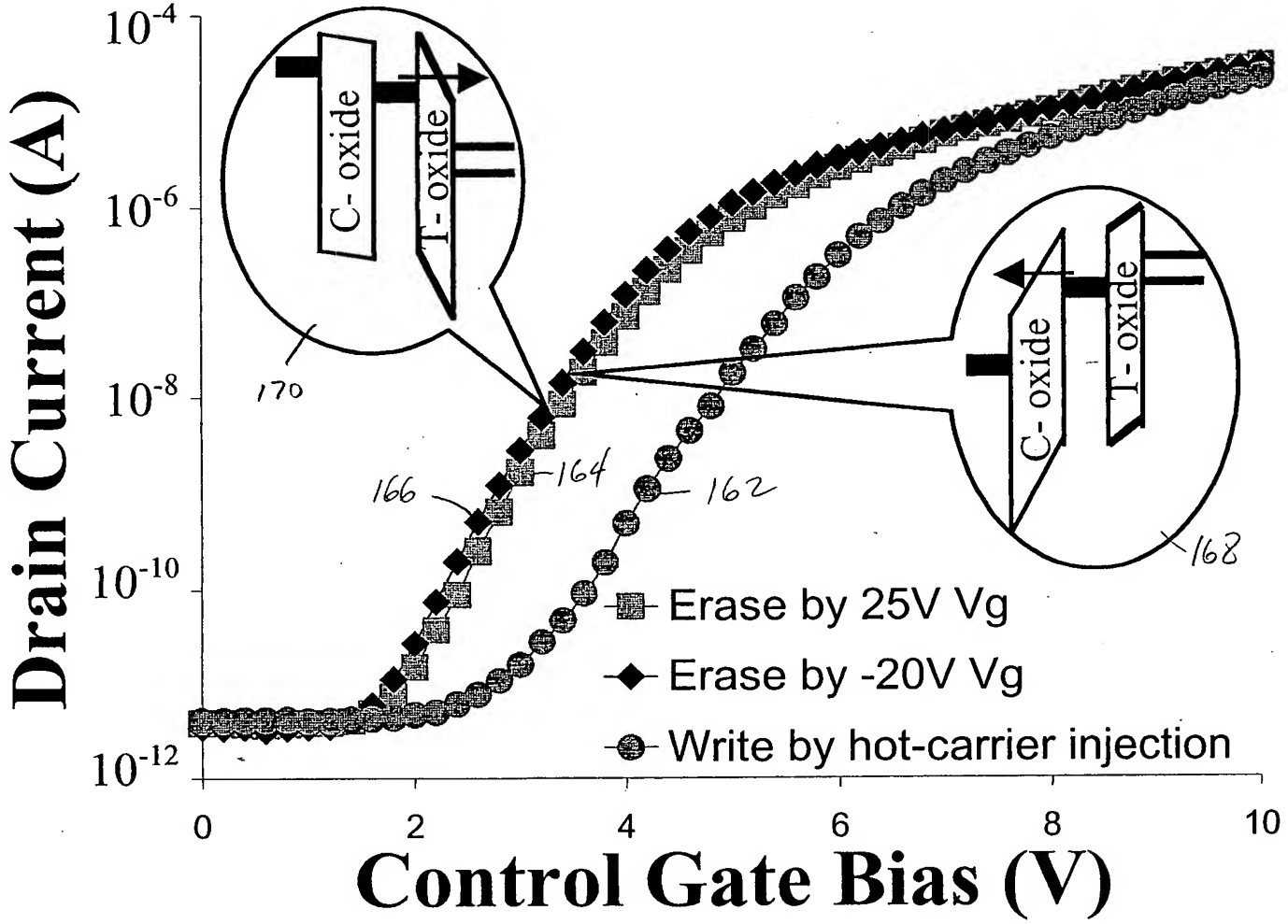

Drain Current (A)
10-4
10-6
10-8
10-10
10-12
0
2
4
6
8
10
Control Gate Bias (V)
C- oxide
T- oxide
170
166
164
162
168
Erase by 25V Vg
Erase by -20V Vg
Write by hot-carrier injection

FIG 19

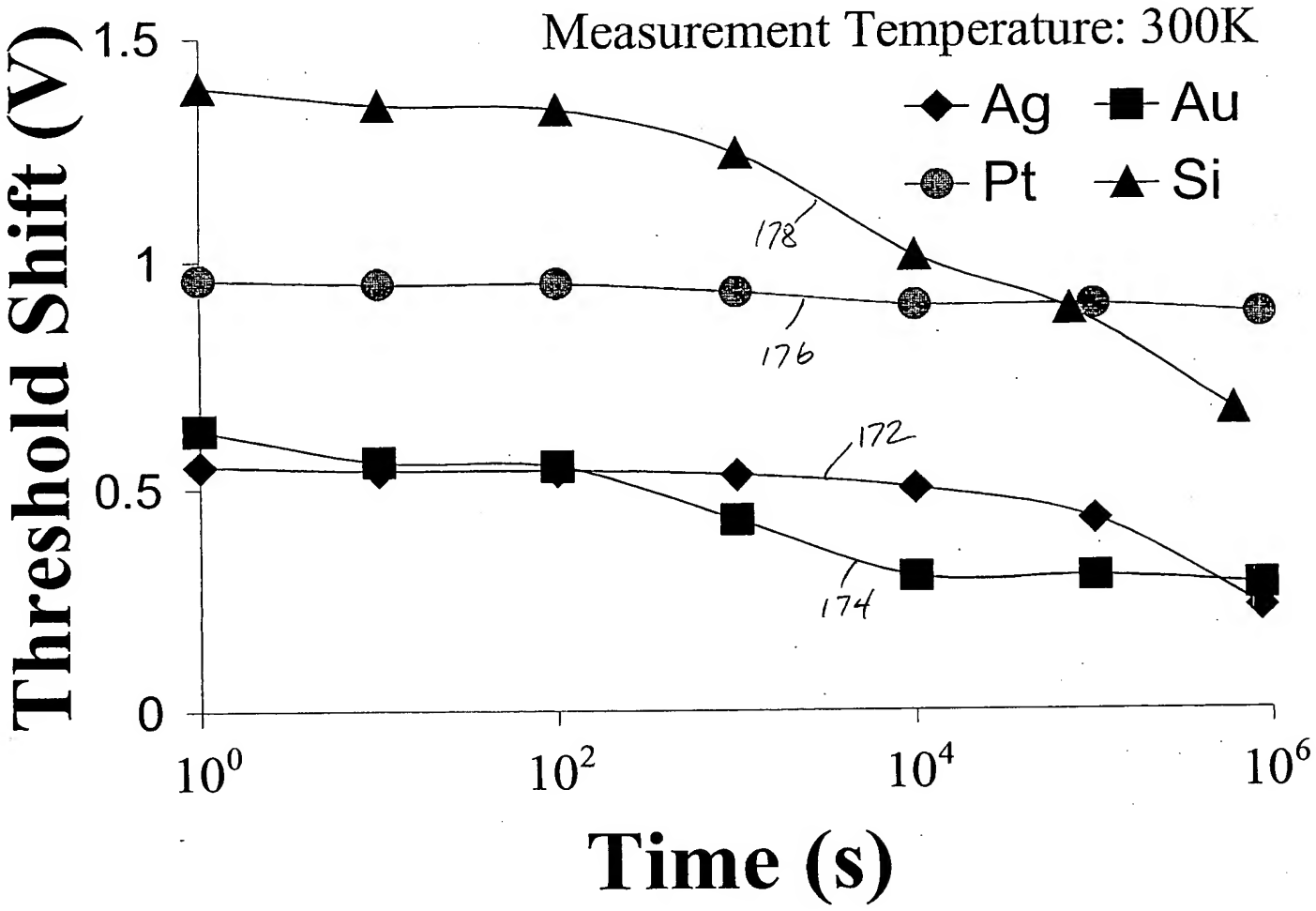
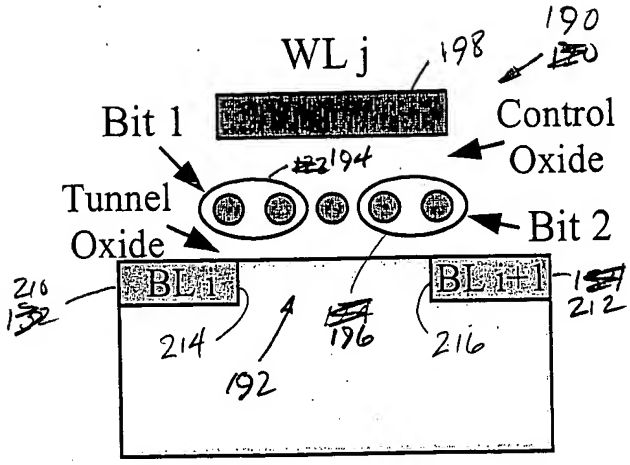
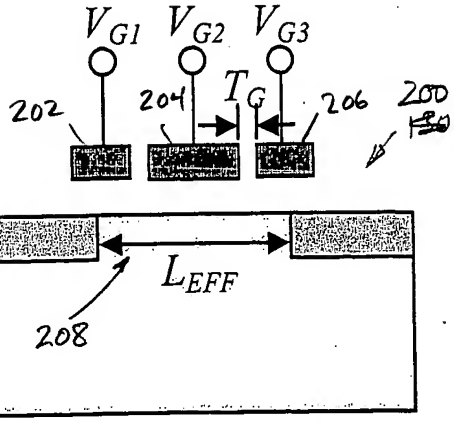

Measurement Temperature: 300K
Ag
Au
Pt
Si
Threshold Shift (V)
1.5
1
0.5
0
10^0
10^2
10^4
10^6
Time (s)
178
176
172
174

FIG 20



Nanocrystal
Memory

FIG. 21(a)



Split-gate
MOSFET

Fig 21(b)

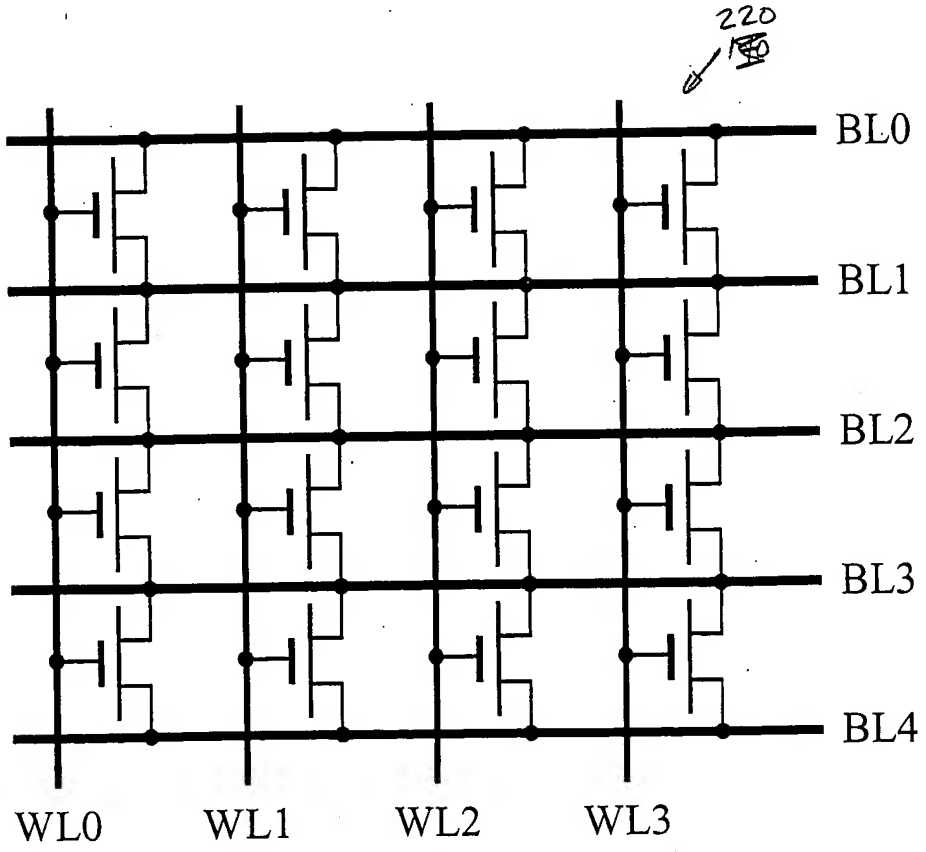


FIG. 21(b)(c)

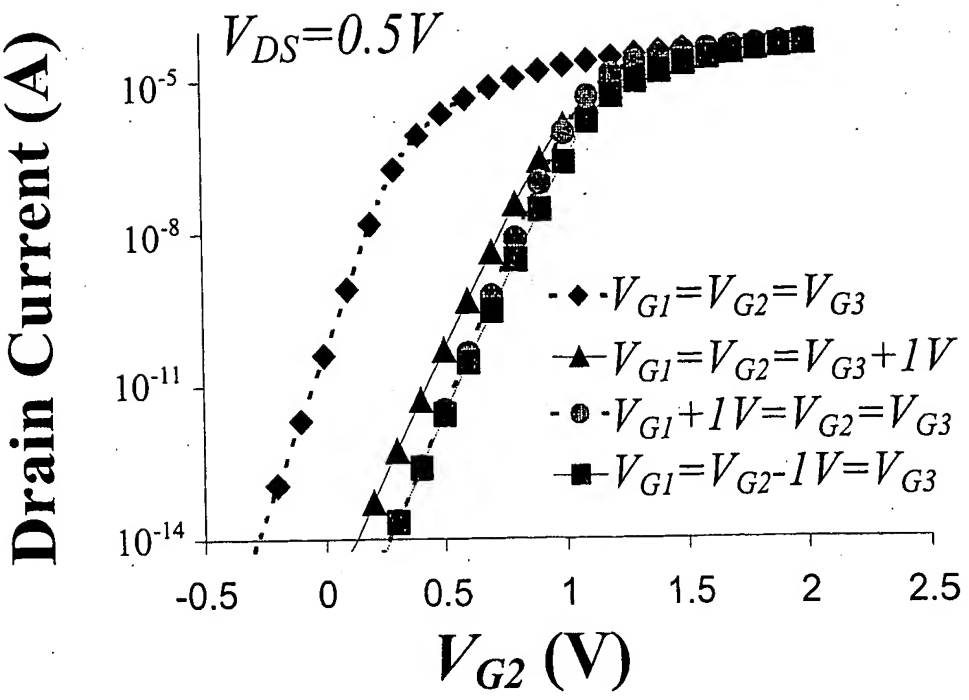


FIG. 22(a)

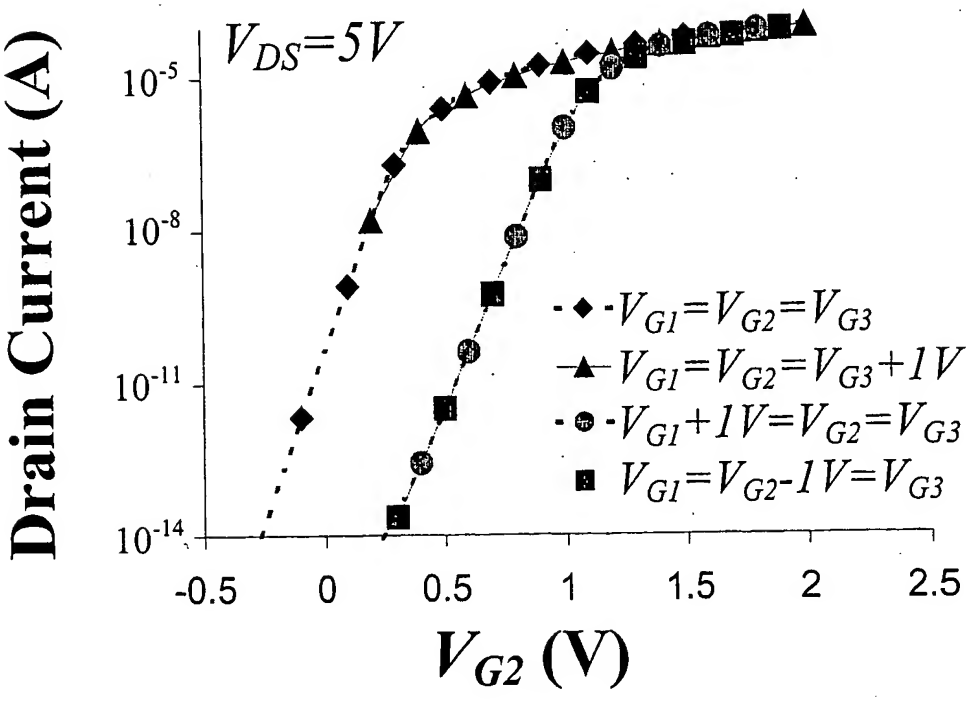


FIG. 22(b)

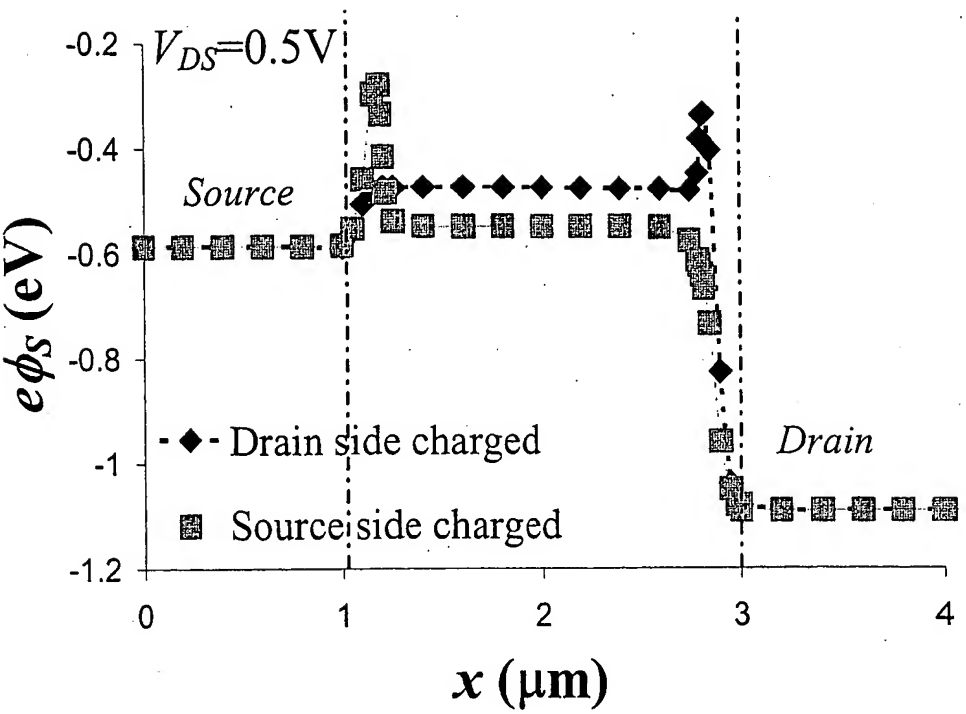


FIG 23(a)

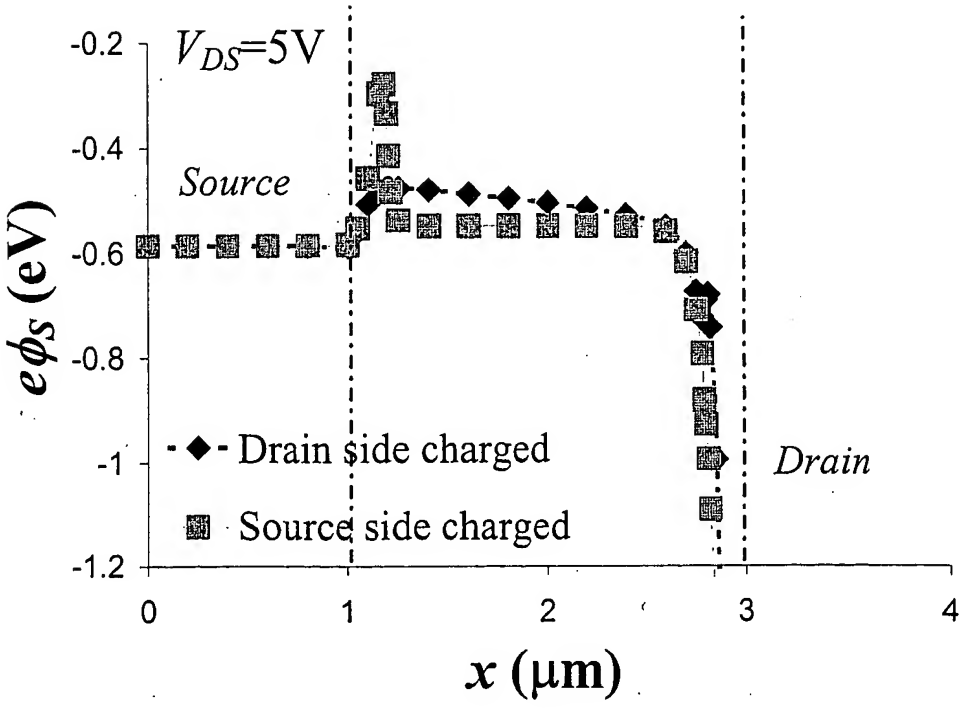


FIG 23(b)

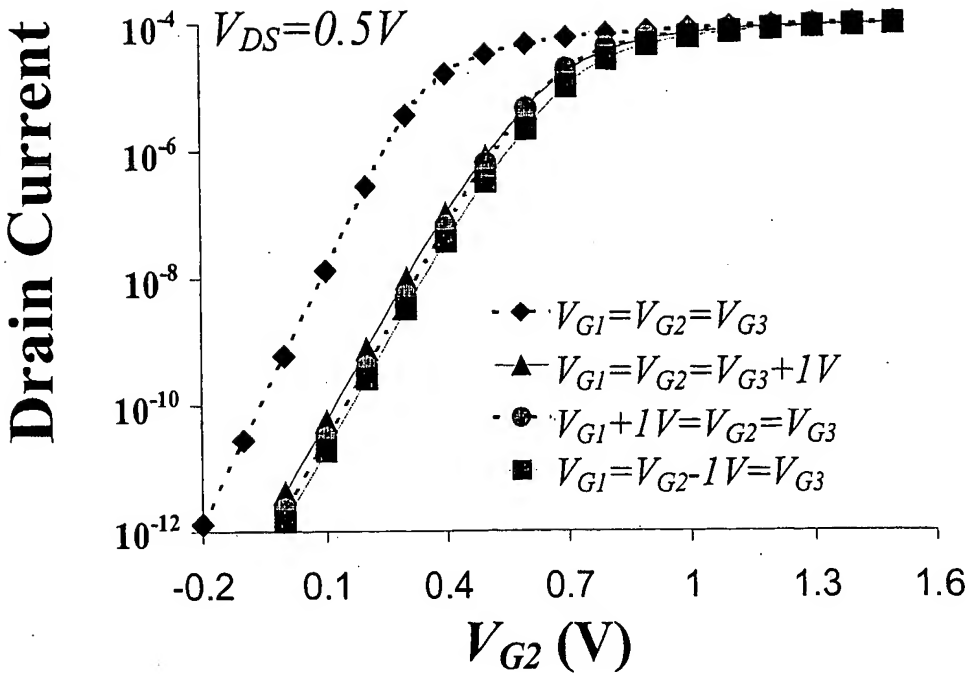


FIG 24(a)

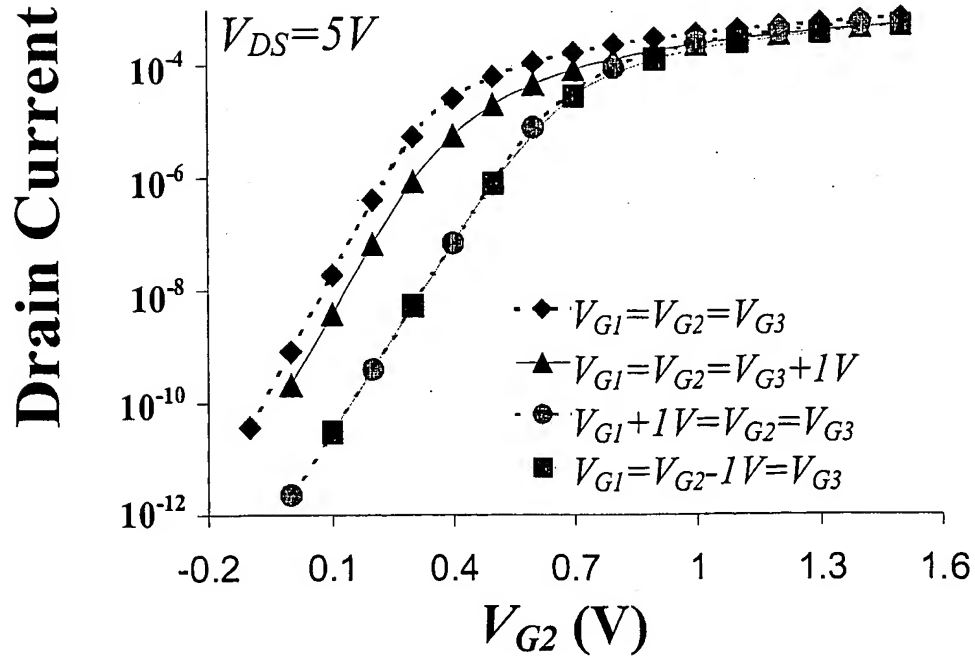


FIG. 24(b)

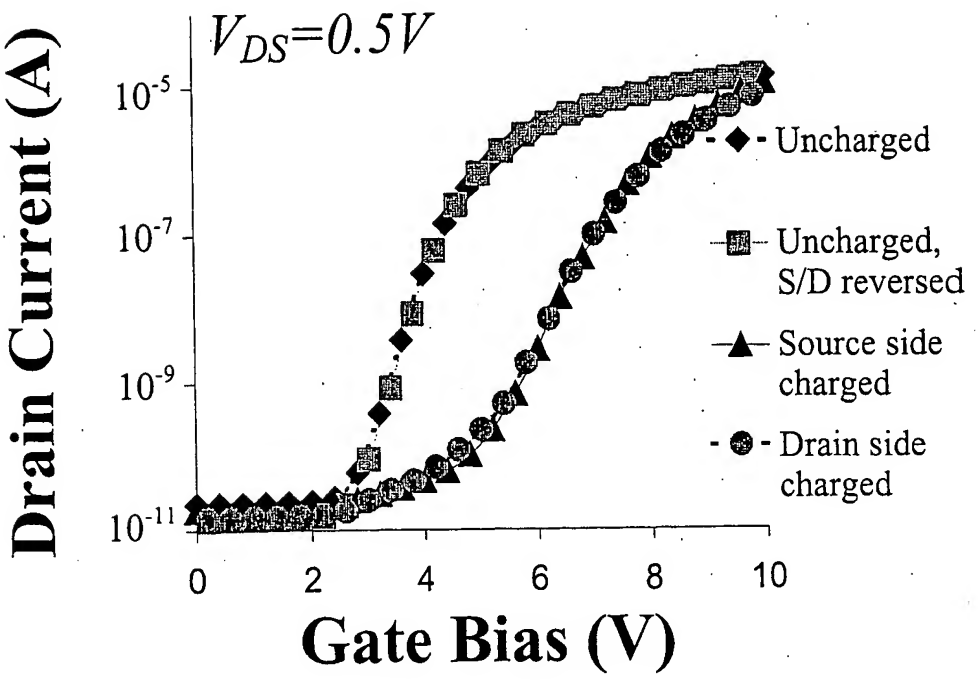


FIG. 25(a)

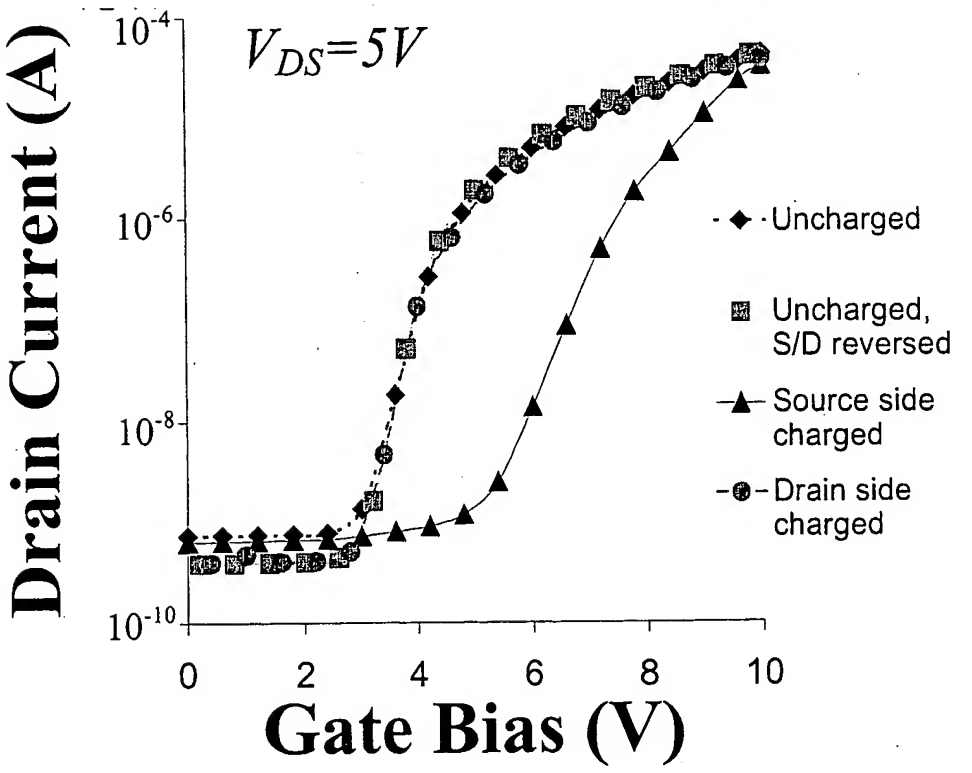
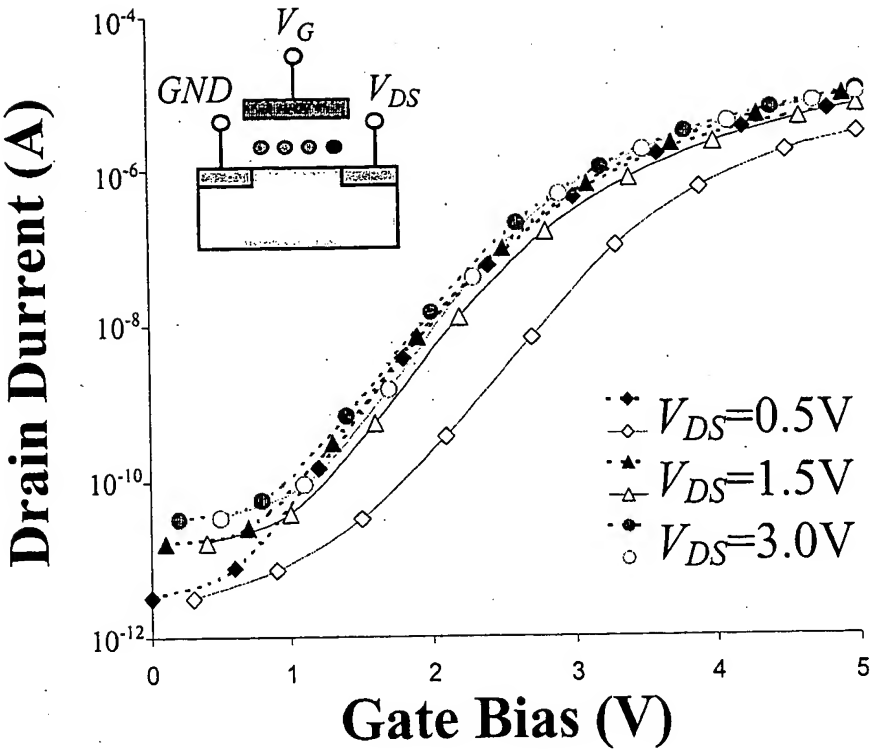
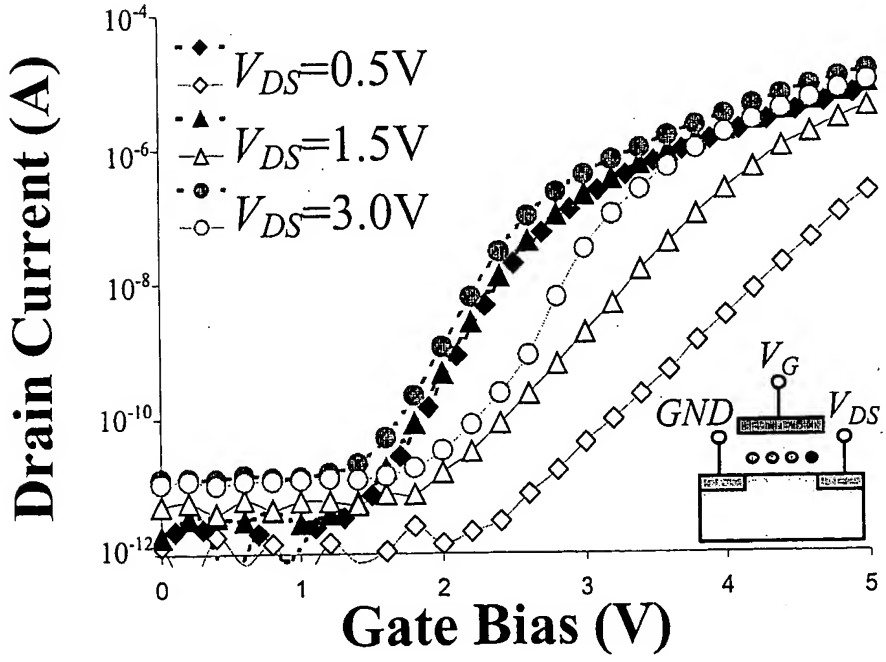


FIG. 25(b)



"Good cell" FIG 26(a)



"Overprogrammed cell"

FIG. 26(b)

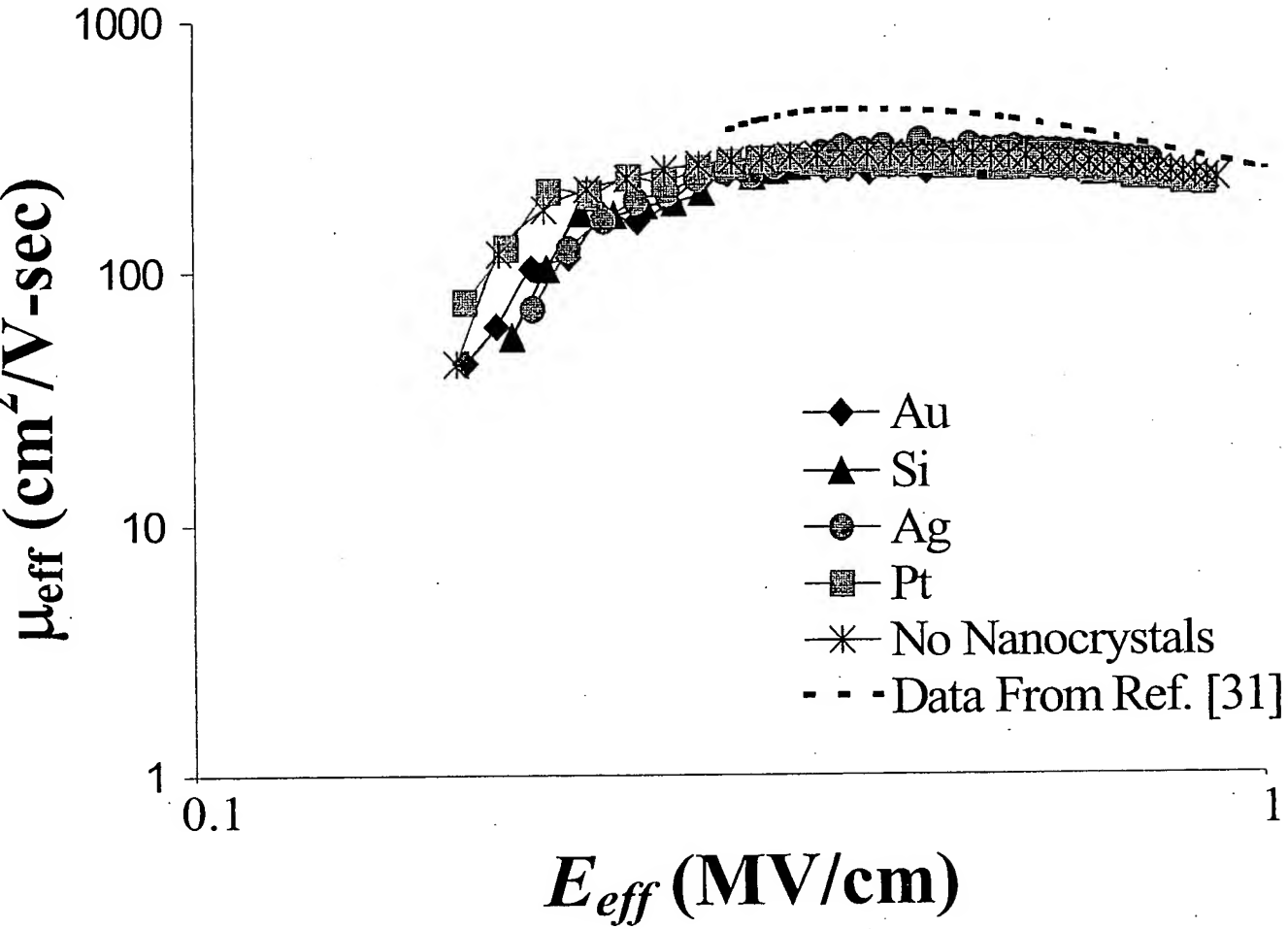

1000
100
10
1
0.1
1
μ_{eff} (cm^2/V-sec)
E_{eff} (MV/cm)
Au
Si
Ag
Pt
No Nanocrystals
Data From Ref. [31]

FIG. 27

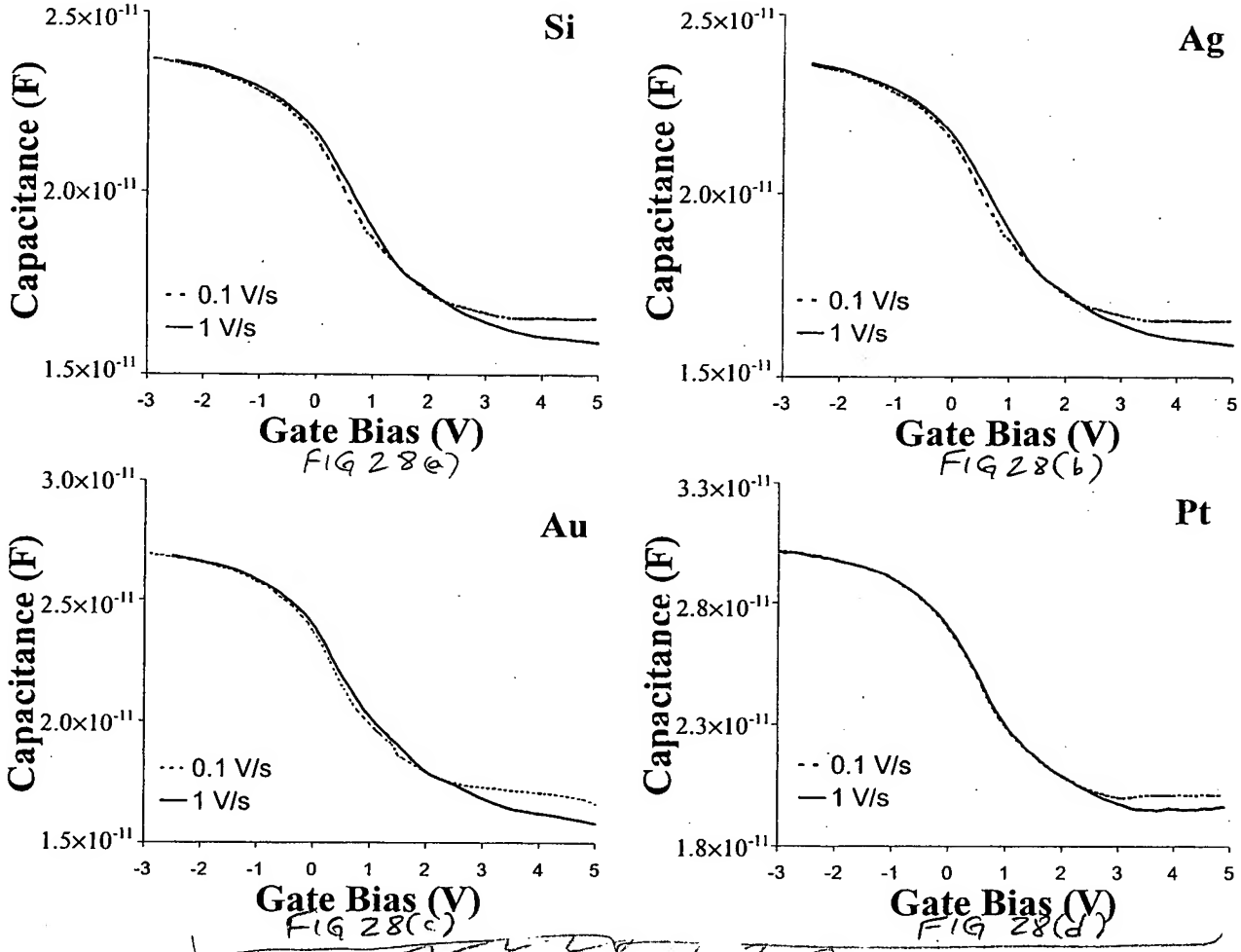

Si
Capacitance (F)
2.5×10-11
2.0×10-11
1.5×10-11
-- 0.1 V/s
— 1 V/s
-3 -2 -1 0 1 2 3 4 5
Gate Bias (V)
FIG 28(a)
Ag
Capacitance (F)
2.5×10-11
2.0×10-11
1.5×10-11
-- 0.1 V/s
— 1 V/s
-3 -2 -1 0 1 2 3 4 5
Gate Bias (V)
FIG 28(b)
Au
Capacitance (F)
3.0×10-11
2.5×10-11
2.0×10-11
1.5×10-11
··· 0.1 V/s
— 1 V/s
-3 -2 -1 0 1 2 3 4 5
Gate Bias (V)
FIG 28(c)
Pt
Capacitance (F)
3.3×10-11
2.8×10-11
2.3×10-11
1.8×10-11
-- 0.1 V/s
— 1 V/s
-3 -2 -1 0 1 2 3 4 5
Gate Bias (V)
FIG 28(d)

FIG 28